


8		7		6		5		4		3		2		1		
1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%. 2. ALL CAPACITANCE VALUES ARE IN MICROFARADS. 3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.												REV	ECN	DESCRIPTION OF REVISION	CK APPD DATE	
															2015-02-12	
J95 MLB SKL EMERALD																
LAST_MODIFICATION=Thu Feb 12 14:48:08 2015																
D	PAGE		<CSA>	CONTENTS		SYNC		DATE		PAGE		<CSA>	CONTENTS		SYNC DATE	
	1		1	SCHEM,K72,MLB ULTIMATE		jerrychow_skl		12/12/2014		61		70	CPU & CHIPSET: CPU CORE VR		samihan_mlb_skl 01/30/2015	
	2		2	BOM Configuration		jerrychow_skl		12/12/2014		62		71	CPU & CHIPSET: CPU CORE VR (VCC)		samihan_mlb_skl 01/30/2015	
	3		3	DEBUG: LEDs		samihan_mlb_skl		01/30/2015		63		72	CPU & CHIPSET: CPU CORE VR (VCCGT)		samihan_mlb_skl 01/30/2015	
	4		4	MECHANICAL: Holes/PD parts		samihan_mlb_skl		01/30/2015		64		73	CPU & CHIPSET: CPU VDDQ VR		samihan_mlb_skl 01/30/2015	
	5		5	CPU & CHIPSET: CPU DMI/PEG/FDI/RSVD		samihan_mlb_skl		01/30/2015		65		75	CPU & CHIPSET: CPU VCCIO VR		samihan_mlb_skl 01/30/2015	
	6		6	CPU & CHIPSET: CPU Clock/Misc/JTAG/CFG		samihan_mlb_skl		01/30/2015		66		76	PLATFORM POWER: 3.3V S5/5V S4 VR		samihan_mlb_skl 01/30/2015	
	7		7	CPU & CHIPSET: DDR3L Interfaces		samihan_mlb_skl		01/30/2015		67		77	CPU & CHIPSET: PCH IVO VR		samihan_mlb_skl 01/30/2015	
	8		8	CPU & CHIPSET: CPU Power		samihan_mlb_skl		01/30/2015		68		78	CPU & CHIPSET: CPU CORE VR (VCCSA)		samihan_mlb_skl 01/30/2015	
	9		9	CPU & CHIPSET: CPU Ground		samihan_mlb_skl		01/30/2015		69		81	DISPLAY: LCD Backlight Driver (LP8565)		samihan_mlb_skl 01/30/2015	
	10		10	CPU & CHIPSET: CPU Decoupling		samihan_mlb_skl		01/30/2015		70		82	DISPLAY: Backlight Driver 2		samihan_mlb_skl 01/30/2015	
	11		11	CPU & CHIPSET: Clocks/HDA/JTAG		samihan_mlb_skl		01/30/2015		71		84	PLATFORM POWER: FET-Controlled S0 and S4		samihan_mlb_skl 01/30/2015	
C	12		12	CPU & CHIPSET: PCH RTC/DMI/PM/CPU_Misc		samihan_mlb_skl		01/30/2015		72		85	PLATFORM POWER: Regulator Enables		samihan_mlb_skl 01/30/2015	
	13		13	CPU & CHIPSET: PCH PCI-E/USB		samihan_mlb_skl		01/30/2015		73		86	PLATFORM POWER: PM Power Good		samihan_mlb_skl 01/30/2015	
	14		14	CPU & CHIPSET: PCH GPIO/Misc		samihan_mlb_skl		01/30/2015		74		87	GFX: Emerald PCIe		samihan_mlb_skl 01/15/2015	
	15		15	CPU & CHIPSET: PCH Power/Decoupling		samihan_mlb_skl		01/30/2015		75		88	GFX: Emerald CORE/FB POWER		samihan_mlb_skl 01/15/2015	
	16		16	CPU & CHIPSET: PCH Grounds		samihan_mlb_skl		01/30/2015		76		90	GFX: Emerald FRAME BUFFER		mlb_hsw_em 12/19/2014	
	17		18	CPU & CHIPSET: XDP		samihan_mlb_skl		01/30/2015		77		92	GDDR5 Frame Buffer A		mlb_hsw_em 12/19/2014	
	18		19	CPU & CHIPSET: Chipset Support		samihan_mlb_skl		01/30/2015		78		93	GDDR5 Frame Buffer B		mlb_hsw_em 12/19/2014	
	19		20	CPU & CHIPSET: Project Chipset Support		samihan_mlb_skl		01/30/2015		79		96	GFX: Emerald IntDP/TBT DP		mlb_hsw_em 12/19/2014	
	20		22	DRAM: VREF/VTT EN		samihan_mlb_skl		01/30/2015		80		97	GFX: Emerald GPIOs,CLK,STRAPS		mlb_hsw_em 12/19/2014	
	21		23	DRAM: SO-DIMM Connector A Slot0		samihan_mlb_skl		01/30/2015		81		99	GFX: Emerald Gnds & Unused		mlb_hsw_em 12/19/2014	
	22		24	DRAM: SO-DIMM Connector A Slot1		samihan_mlb_skl		01/30/2015		82		101	GRAPHICS: GPU CORE VR		mlb_hsw_em 12/19/2014	
	23		25	DRAM: SO-DIMM CONNECTOR B SLOT0		samihan_mlb_skl		01/30/2015		83		102	GRAPHICS: GPU CORE VR (PHASES 1-3)		mlb_hsw_em 12/19/2014	
B	24		26	DRAM: SO-DIMM CONNECTOR B SLOT1		samihan_mlb_skl		01/30/2015		84		103	GRAPHICS: GPU CORE VR (PHASES 4-6)		samihan_mlb_skl 01/30/2015	
	25		27	DRAM: ALIASES AND BITSWAPS		samihan_mlb_skl		01/30/2015		85		104	GRAPHICS: GPU VDDQ VR		samihan_mlb_skl 01/30/2015	
	26		28	TBT/DP: Host (1 of 2)		samihan_mlb_skl		01/30/2015		86		105	GRAPHICS: GPU VDDCI VR		samihan_mlb_skl 01/30/2015	
	27		29	TBT/DP: Host (2 of 2)		samihan_mlb_skl		01/30/2015		87		106	GRAPHICS: GPU OV95 VR		samihan_mlb_skl 01/30/2015	
	28		30	Thunderbolt: Power Support		samihan_mlb_skl		01/15/2015		88		107	GRAPHICS: GPU IVO VR		samihan_mlb_skl 01/30/2015	
	29		32	TBT/DP: Connector A		samihan_mlb_skl		01/30/2015		89		109	Power Connectors/Aliases		samihan_mlb_skl 01/30/2015	
	30		33	TBT/DP: Connector B		samihan_mlb_skl		01/30/2015		90		110	Signal Aliases		samihan_mlb_skl 02/02/2015	
	31		34	TBT/DP: DDC Crossbar		samihan_mlb_skl		01/30/2015		91		111	Unused Signal Aliases		mlb_hsw_em 12/19/2014	
	32		35	WIRELESS: Airport/Bluetooth		samihan_mlb_skl		01/30/2015		92		112	J95 RULE DEFINITIONS		mlb_hsw_em 12/19/2014	
	33		37	SDD/HDD:SATA/SSD Connectors		samihan_mlb_skl		01/30/2015		93		113	J95 RULE DEFINITIONS		mlb_hsw_em 12/19/2014	
	34		38	HDD: SSD Temp Sense		samihan_mlb_skl		01/30/2015				114			mlb_hsw_em 12/19/2014	
	35		39	ETHERNET: PHY (CAESAR IV)		samihan_mlb_skl		01/30/2015				119			mlb_hsw_em 12/19/2014	
A	36		40	ETHERNET: Support & Connector		samihan_mlb_skl		01/30/2015				120			jerrychow_skl 12/12/2014	
	37		41	SD CARD: Connector		samihan_mlb_skl		01/30/2015							jerrychow_skl 12/12/2014	
	38		42	CAMERA: Controller		samihan_mlb_skl		01/30/2015							jerrychow_skl 12/12/2014	
	39		43	CAMERA: Controller Support		samihan_mlb_skl		01/30/2015							jerrychow_skl 12/12/2014	
	40		44	DISPLAY: Support		samihan_mlb_skl		01/30/2015							jerrychow_skl 12/12/2014	
	41		45	DISPLAY: MUXing		samihan_mlb_skl		01/30/2015								
	42		46	USB-A: EXTERNAL USB PORTS A & B		samihan_mlb_skl		01/30/2015								
	43		47	USB-A: EXTERNAL USB PORTS C & D		samihan_mlb_skl		01/30/2015								
	44		50	SMC: Controller		samihan_mlb_skl		01/30/2015								
	45		51	SMC: Controller Support		samihan_mlb_skl		01/30/2015								
	46		52	CPU & CHIPSET: SPI and Debug Connector		samihan_mlb_skl		01/30/2015								
	47		53	SMC: SMBus Connections		samihan_mlb_skl		01/30/2015								
48		54	SENSORS: I and V Sense		samihan_mlb_skl		01/30/2015									
49		55	SENSORS: I and V Sense(Continued)		samihan_mlb_skl		01/30/2015									
50		56	SENSORS: Temperature Sensors		samihan_mlb_skl		01/30/2015									
51		60	FAN: System Fan		samihan_mlb_skl		01/30/2015									
52		61	AUDIO: CODEC/REGULATORS		samihan_mlb_skl		01/30/2015									
53		62	AUDIO: HEADPHONE AMP		samihan_mlb_skl		01/30/2015									
54		63	AUDIO: LEFT SPKR AMP		samihan_mlb_skl		01/30/2015									
55		64	AUDIO: RIGHT SPKR AMP		samihan_mlb_skl		01/30/2015									
56		65	AUDIO: Jack, Mikey, CHS Switch		samihan_mlb_skl		01/30/2015									
57		66	Audio: Spkr/Mic Conn.		samihan_mlb_skl		01/30/2015									
58		67	AUDIO: Detects/Grounding		samihan_mlb_skl		01/30/2015									
59		68	AUDIO: Speaker ID		samihan_mlb_skl		01/30/2015									
60		69	PLATFORM POWER: Connectors / VReg G3Hot		samihan_mlb_skl		01/30/2015									
SCHEM,J95, mlb_skl_EM																
DRAWING TITLE																
SCHEM,MLB,SKYLAKE,EMERALD,J95																
 Apple Inc.												DRAWING NUMBER		SIZE		
												051-00673		D		
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												PAGE		1 OF 121		
												SHEET		1 OF 93		

8		7		6		5		4		3		2		1																																																																																																											
D	BOM Variants															D																																																																																																									
	<table><tr><th>BOM NUMBER</th><th colspan="4">BOM NAME</th><th colspan="10">BOM OPTIONS</th></tr><tr><td>985-00098</td><td colspan="4">PCBA, DEV, MLB_SKL, J95</td><td colspan="10">DEVELOPMENT, J95_DEVEL</td></tr><tr><td>685-00062</td><td colspan="4">PCBA, MLB_SKL, COMMON PARTS, J95</td><td colspan="10">J95_COMMON</td></tr><tr><td>639-00957</td><td colspan="4">PCBA, MLB_SKL, EMERALD_PROA, VRAM_HYNIX, 2GB, J95</td><td colspan="10">J95, MLB_CNNPTS, CPU: BEST, SSD: Y, GPU: EMERALD_PROA, FB: 4G_HYNIX, EEEE: GHN4</td></tr><tr><td>639-00959</td><td colspan="4">PCBA, MLB_SKL, EMERALD_PROA, VRAM_ELPIDA, 2GB, J95</td><td colspan="10">J95, MLB_CNNPTS, CPU: BEST, SSD: Y, GPU: EMERALD_PROA, FB: 4G_ELPIDA, EEEE: GHN5</td></tr><tr><td>639-01039</td><td colspan="4">PCBA, MLB_SKL, 95W, EMERALD_PROA, VRAM_HYNIX, 2GB, J95</td><td colspan="10">J95, MLB_CNNPTS, CPU: CTO_2.6G, SSD: Y, GPU: EMERALD_PROA, FB: 4G_HYNIX, EEEE: GKCT</td></tr><tr><td>639-01040</td><td colspan="4">PCBA, MLB_SKL, 95W, EMERALD_PROA, VRAM_ELPIDA, 2GB, J95</td><td colspan="10">J95, MLB_CNNPTS, CPU: CTO_2.6G, SSD: Y, GPU: EMERALD_PROA, FB: 4G_ELPIDA, EEEE: GKCV</td></tr></table>																BOM NUMBER	BOM NAME				BOM OPTIONS										985-00098	PCBA, DEV, MLB_SKL, J95				DEVELOPMENT, J95_DEVEL										685-00062	PCBA, MLB_SKL, COMMON PARTS, J95				J95_COMMON										639-00957	PCBA, MLB_SKL, EMERALD_PROA, VRAM_HYNIX, 2GB, J95				J95, MLB_CNNPTS, CPU: BEST, SSD: Y, GPU: EMERALD_PROA, FB: 4G_HYNIX, EEEE: GHN4										639-00959	PCBA, MLB_SKL, EMERALD_PROA, VRAM_ELPIDA, 2GB, J95				J95, MLB_CNNPTS, CPU: BEST, SSD: Y, GPU: EMERALD_PROA, FB: 4G_ELPIDA, EEEE: GHN5										639-01039	PCBA, MLB_SKL, 95W, EMERALD_PROA, VRAM_HYNIX, 2GB, J95				J95, MLB_CNNPTS, CPU: CTO_2.6G, SSD: Y, GPU: EMERALD_PROA, FB: 4G_HYNIX, EEEE: GKCT										639-01040	PCBA, MLB_SKL, 95W, EMERALD_PROA, VRAM_ELPIDA, 2GB, J95				J95, MLB_CNNPTS, CPU: CTO_2.6G, SSD: Y, GPU: EMERALD_PROA, FB: 4G_ELPIDA, EEEE: GKCV									
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	639-00957	PCBA, MLB_SKL, EMERALD_PROA, VRAM_HYNIX, 2GB, J95				J95, MLB_CNNPTS, CPU: BEST, SSD: Y, GPU: EMERALD_PROA, FB: 4G_HYNIX, EEEE: GHN4																																																																																																																			
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	639-01039	PCBA, MLB_SKL, 95W, EMERALD_PROA, VRAM_HYNIX, 2GB, J95				J95, MLB_CNNPTS, CPU: CTO_2.6G, SSD: Y, GPU: EMERALD_PROA, FB: 4G_HYNIX, EEEE: GKCT																																																																																																																			
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34380616	1	IC, BCM57766A1, ENET4S0, 8X8	U3900	CRITICAL																																																																																																																					
Programmable Parts																																																																																																																									
<table><tr><th>PART#</th><th>QTY</th><th>DESCRIPTION</th><th>REFERENCE DESIGNATOR(S)</th><th>CRITICAL</th><th>BOM OPTION</th></tr><tr><td>341800058</td><td>1</td><td>IC, EFI, V0174, J78</td><td>U5210</td><td>CRITICAL</td><td>BOOTROM: PROG</td></tr><tr><td>335800006</td><td>1</td><td>IC, 64 MBIT SPI SERIAL FLASH</td><td>U5210</td><td>CRITICAL</td><td>BOOTROM: BLANK</td></tr><tr><td>341800262</td><td>1</td><td>IC, SMC-B1, EXTERNAL, VXXX, POC-S, J78AM</td><td>U5000</td><td>CRITICAL</td><td>SMC: PROG</td></tr><tr><td>33881214</td><td>1</td><td>IC, SMC12-B1, 4096B/500K1P5, MCI, 1578GA</td><td>U5000</td><td>CRITICAL</td><td>SMC: BLANK</td></tr><tr><td>341800152</td><td>1</td><td>IC, T29, EPROM, FR, VTBD, POC, J95</td><td>U2890</td><td>CRITICAL</td><td>TBTRM: PROG</td></tr><tr><td>33580915</td><td>1</td><td>IC, SRL SPI FLASH ROM, 4MBIT, 5098B, US088</td><td>U2890</td><td>CRITICAL</td><td>TBTRM: BLANK</td></tr><tr><td>34183912</td><td>1</td><td>IC, ENET ROM, NUMONIX, V1.15, J16/J16G/J17</td><td>U3990</td><td>CRITICAL</td><td>CIVROM: PROG</td></tr><tr><td>33580854</td><td>1</td><td>1-MBIT SPI FLASH ROM 501C, HF</td><td>U3990</td><td>CRITICAL</td><td>CIVROM: BLANK</td></tr><tr><td>34183778</td><td>1</td><td>IC, CAMERA_FLASH, V7230, J16/J17</td><td>U4202</td><td>CRITICAL</td><td>CAMROM: PROG</td></tr><tr><td>33580852</td><td>1</td><td>IC, FLASH, SPI, 1MBIT, 3V3</td><td>U4202</td><td>CRITICAL</td><td>CAMROM: BLANK</td></tr></table>															PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION	341800058	1	IC, EFI, V0174, J78	U5210	CRITICAL	BOOTROM: PROG	335800006	1	IC, 64 MBIT SPI SERIAL FLASH	U5210	CRITICAL	BOOTROM: BLANK	341800262	1	IC, SMC-B1, EXTERNAL, VXXX, POC-S, J78AM	U5000	CRITICAL	SMC: PROG	33881214	1	IC, SMC12-B1, 4096B/500K1P5, MCI, 1578GA	U5000	CRITICAL	SMC: BLANK	341800152	1	IC, T29, EPROM, FR, VTBD, POC, J95	U2890	CRITICAL	TBTRM: PROG	33580915	1	IC, SRL SPI FLASH ROM, 4MBIT, 5098B, US088	U2890	CRITICAL	TBTRM: BLANK	34183912	1	IC, ENET ROM, NUMONIX, V1.15, J16/J16G/J17	U3990	CRITICAL	CIVROM: PROG	33580854	1	1-MBIT SPI FLASH ROM 501C, HF	U3990	CRITICAL	CIVROM: BLANK	34183778	1	IC, CAMERA_FLASH, V7230, J16/J17	U4202	CRITICAL	CAMROM: PROG	33580852	1	IC, FLASH, SPI, 1MBIT, 3V3	U4202	CRITICAL	CAMROM: BLANK																																									
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155S0830	155S0316		ALL	1000																																																																																																																					

Bar Code Labels / EEEE #'s

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
825-7896	1	LABEL, MLB, 2D	EEEE_GHN4	CRITICAL	EEEE:GHN4
825-7896	1	LABEL, MLB, 2D	EEEE_GHN5	CRITICAL	EEEE:GHN5
825-7896	1	LABEL, MLB, 2D	EEEE_GHN4	CRITICAL	EEEE:GKCT
825-7896	1	LABEL, MLB, 2D	EEEE_GHN5	CRITICAL	EEEE:GKCV

J95 SCHEMATIC / PCB #'S


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-00673	1	SCH, MLB SKL EM, J95	SCH1	CRITICAL	J95
820-00291	1	PCBF, MLB SKL EM, J95	PCB1	CRITICAL	J95
685-00062	1	PCBA, MLB SKL EM COMMON PARTS, J95	CNNPTS	CRITICAL	MLB_CNNPTS

J95 ALTERNATES

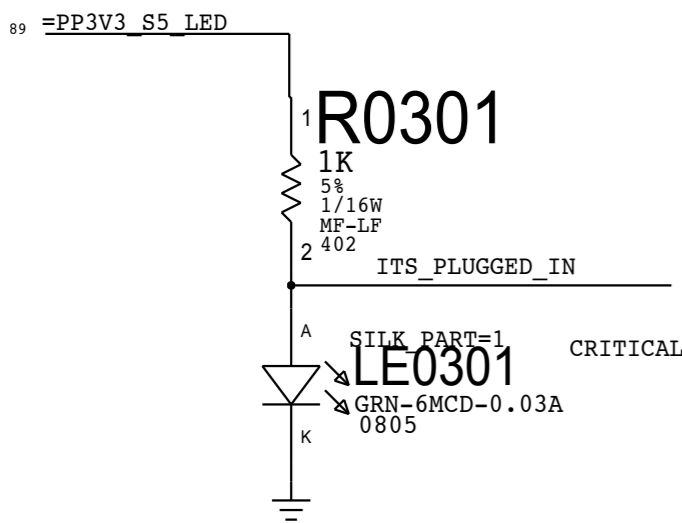
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
377S0147	377S0126		ALL	USB Diode Array
197S0481	197S0480		ALL	25MHX PCH XTAL
197S0479	197S0478		ALL	12MHZ CAM/XXP XTAL
372S0186	372S0185		ALL	Alternate Temp Diode
107S00030	107S00029		ALL	Alt 5mOhm sense
107S0255	107S0240		ALL	Alt 1mOhm sense
341S00016	341S3912		U3990	IC, ENETROM, ADESTO, V1.15, J78
138S0681	138S0638		ALL	10uF Caps
138S0860	138S0775		ALL	Single-source 1uF 402
128S0398	128S0220		ALL	3.3V INPUT CAP
378S0391	378S0390		ALL	DEGUG LEDS
311S00008	311S0271		ALL	AND GATE
155S0830	155S0316		ALL	EEP ROM, 64K, 0.1, 1.44
376S00016	376S0644		ALL	MOSFET, P-CH, 20V, 1A
376S00001	376S0659		ALL	MOSFET, P-CH, 20V
376S00015	376S0610		ALL	XSTR, FET, DL NCH, 60V
138S1103	138S0719		ALL	4.7uF 0402
311S00004	311S0370		ALL	Config. Logic Gate
311S0250	311S0377		ALL	AND GATE
132S0447	132S0448		ALL	0.1uF 0201
138S0855	138S0750		ALL	4.7uF 0402
353S00095	353S3328		ALL	2:4 Diff MUX
311S00072	311S0657		ALL	Dual 2 INP AND GATE

GPU and VRAM

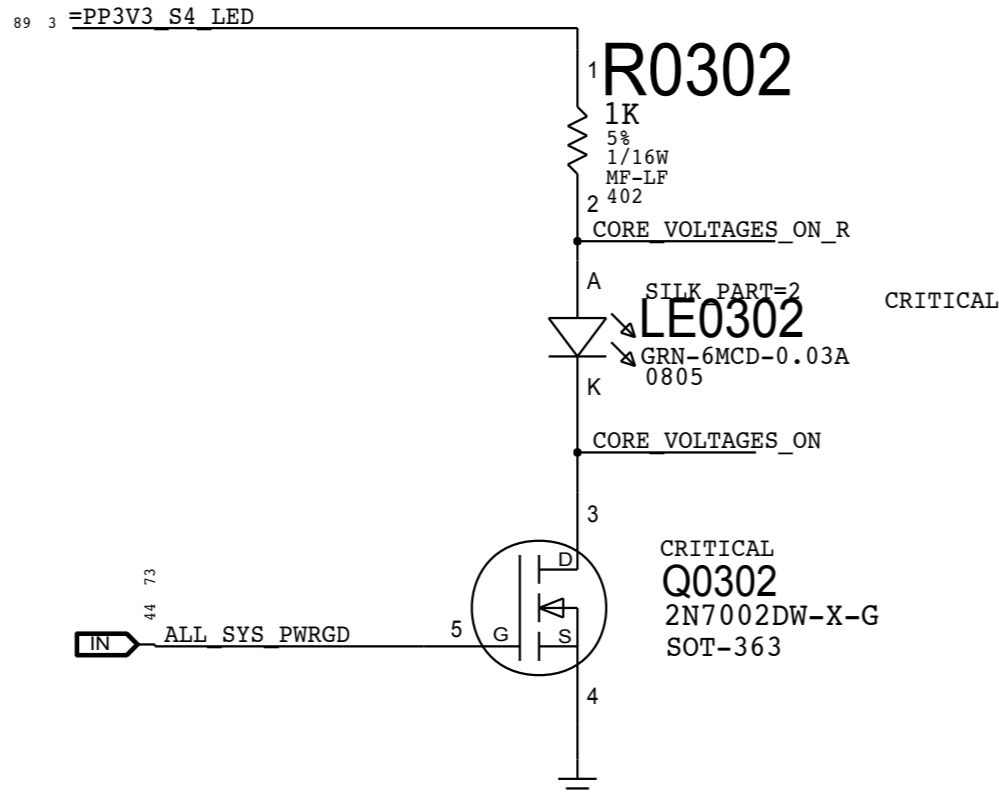
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333800043	4	IC, EYX, GDDR5, 4GBIT, 64MX32, 7GBPS, 25NM	U9200, U9250, U9300, U9350	CRITICAL	FB: 4G_HYNIX
333800044	4	IC, ELP, GDDR5, 4GBIT, 64MX32, 7GBPS, 25NM	U9200, U9250, U9300, U9350	CRITICAL	FB: 4G_ELPIDA

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PAGE TITLE			
BOM Configuration			
 Apple Inc.		DRAWING NUMBER	051-00673
		REVISION	0.24.0
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		PAGE	2 OF 121
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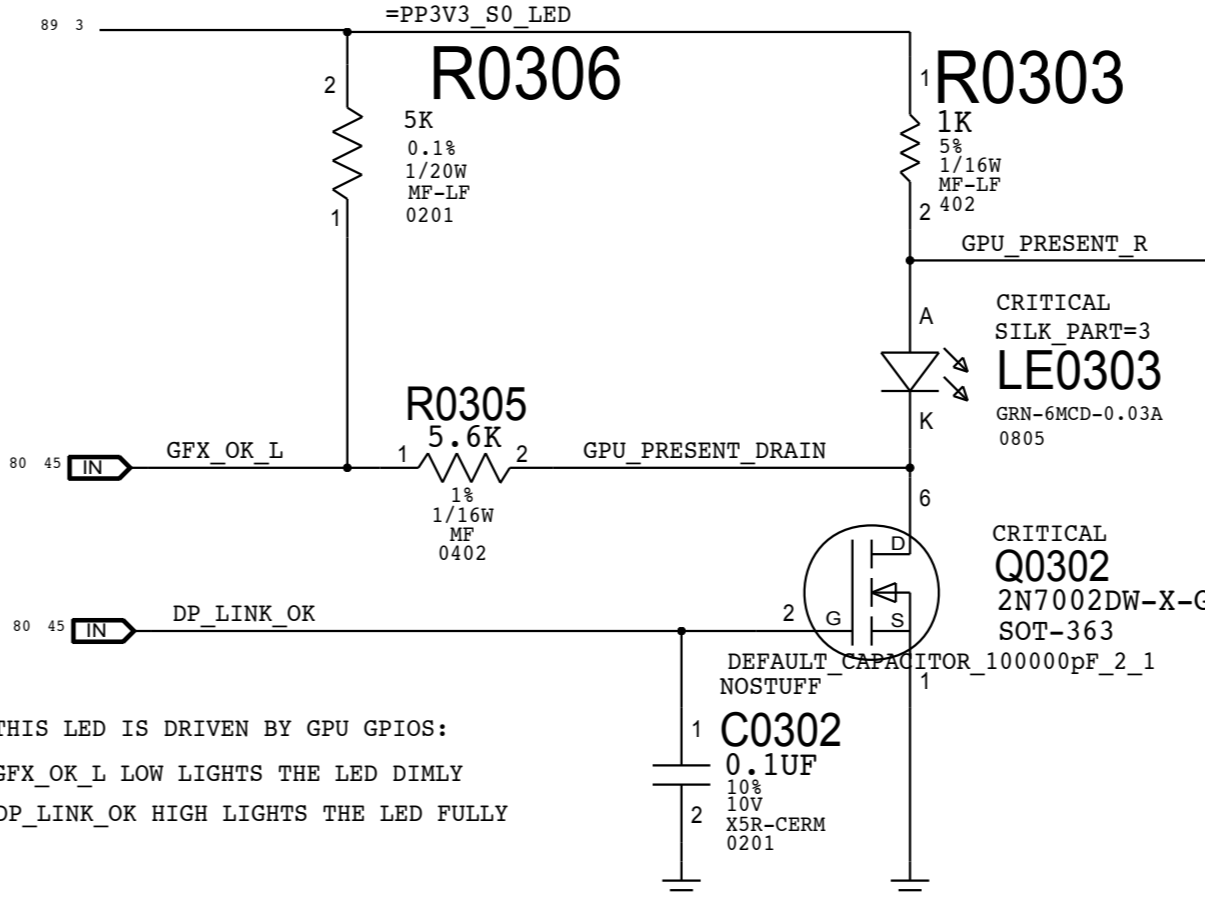
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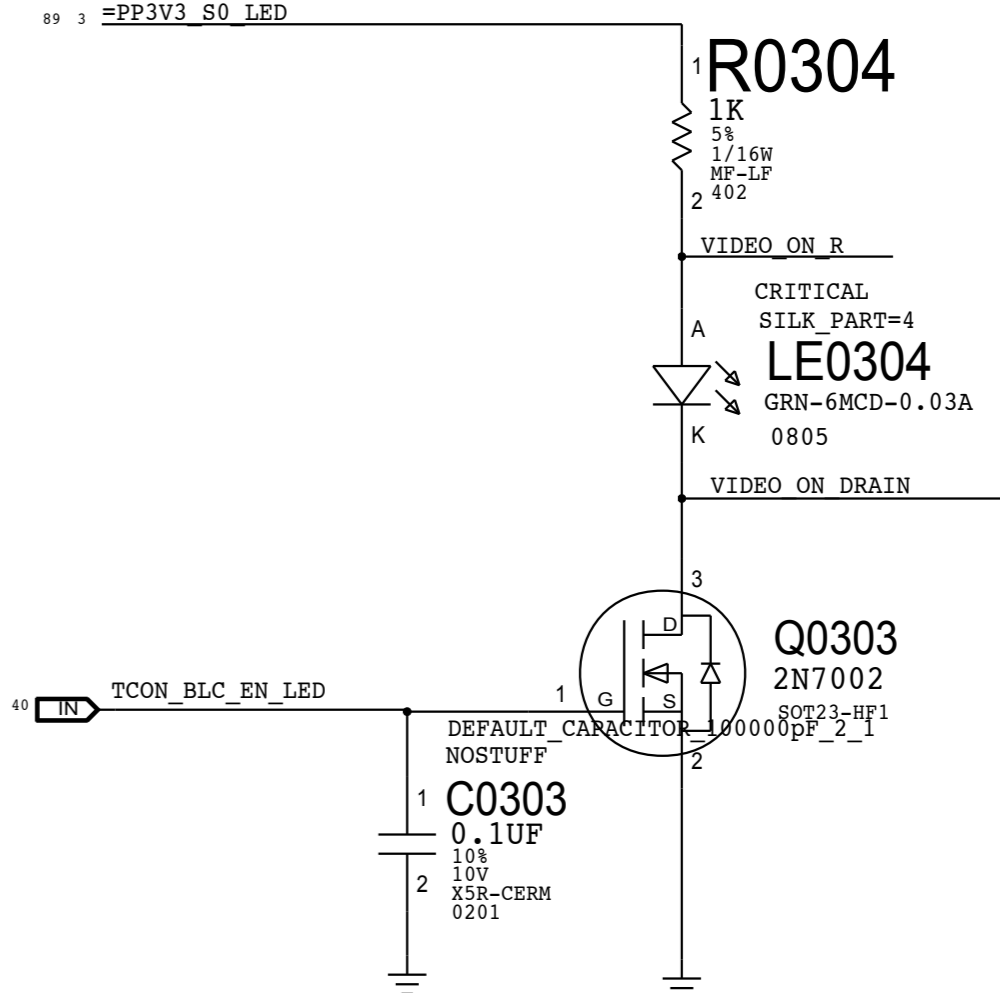
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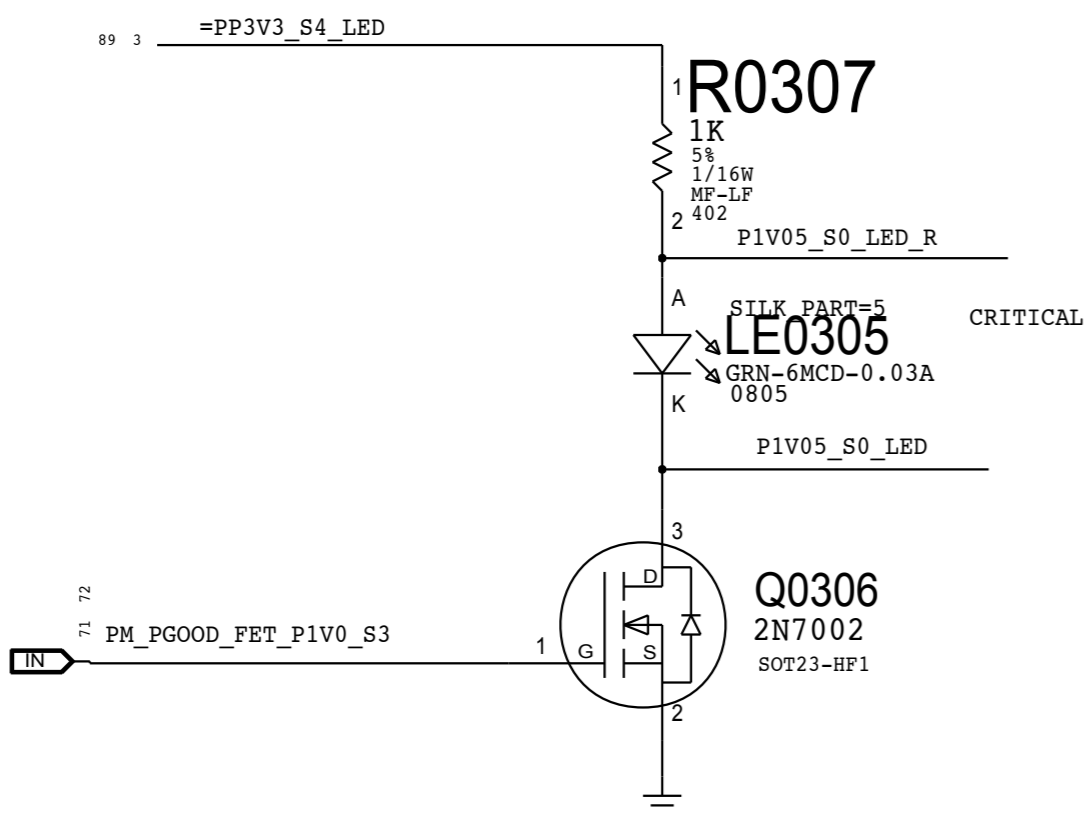
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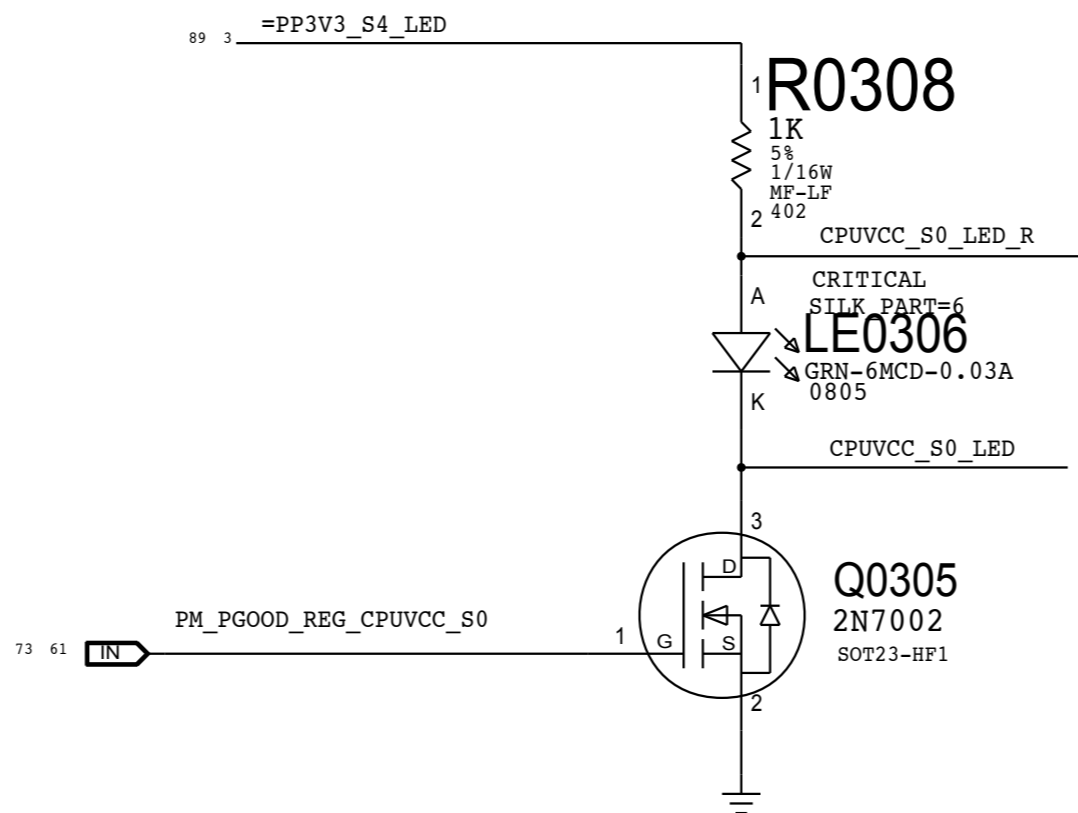
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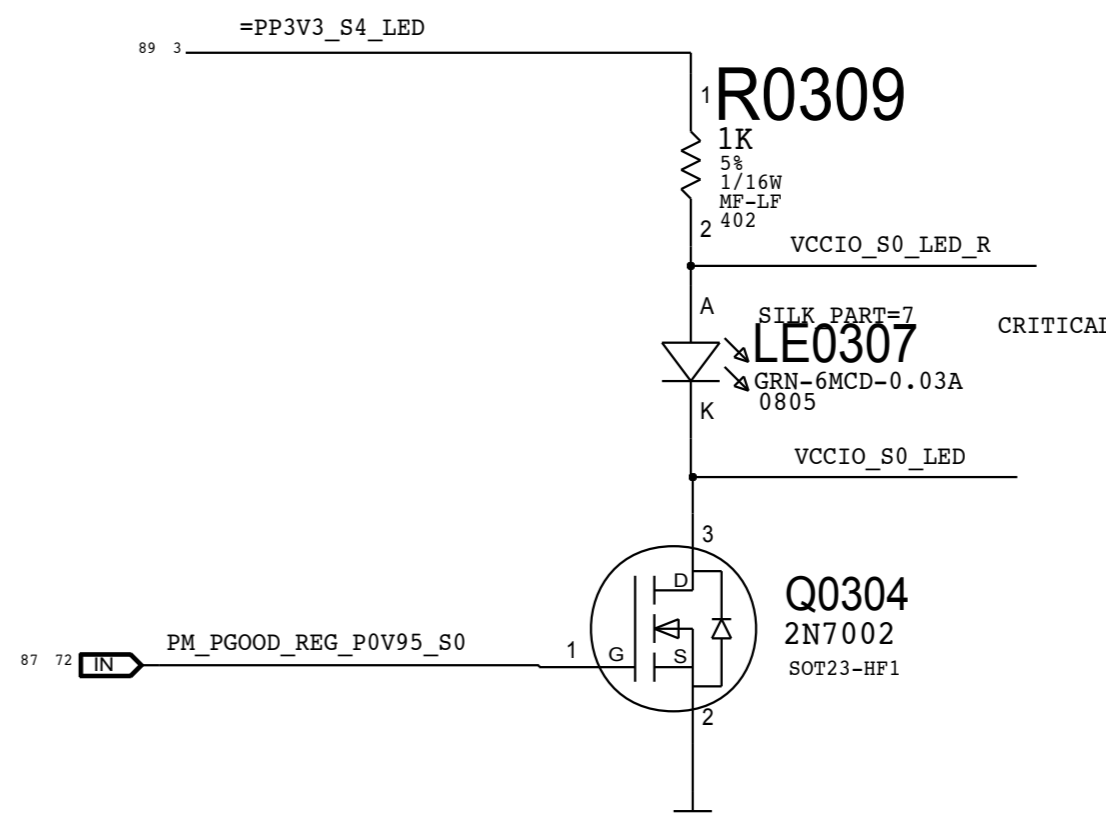
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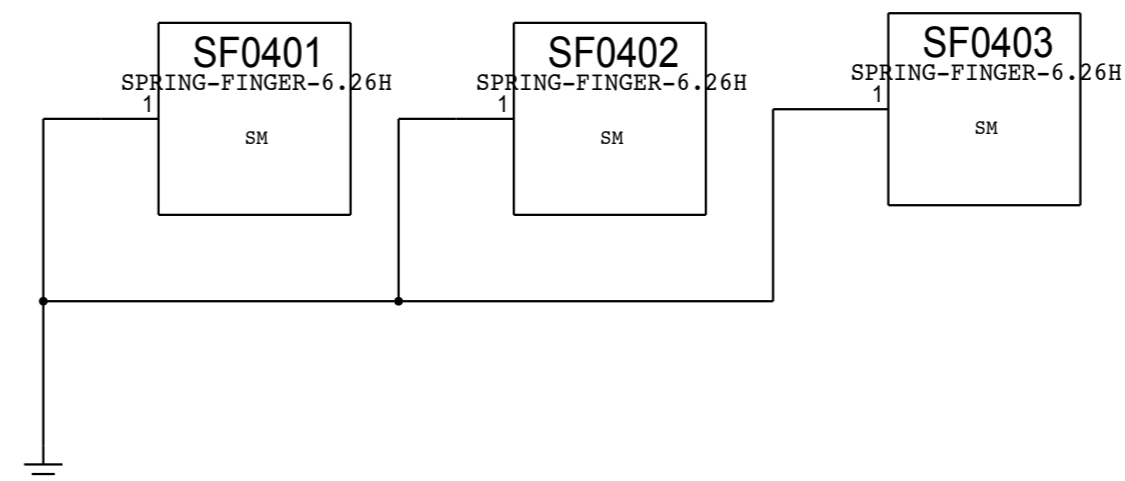
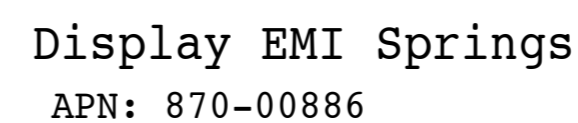
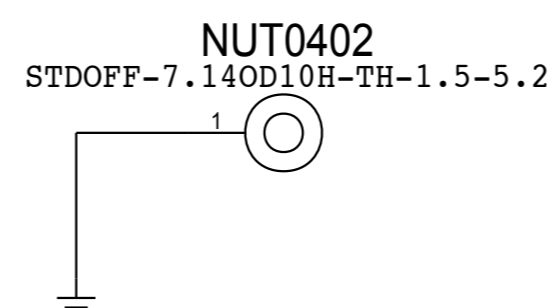
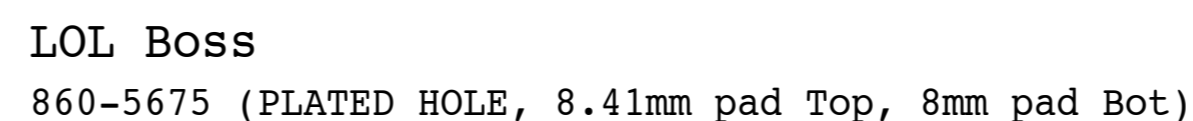
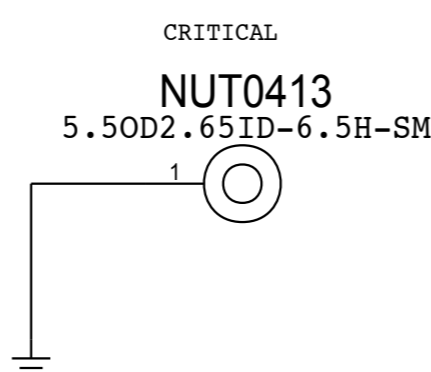
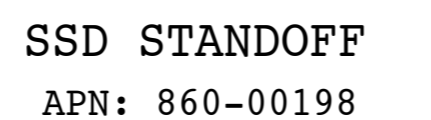
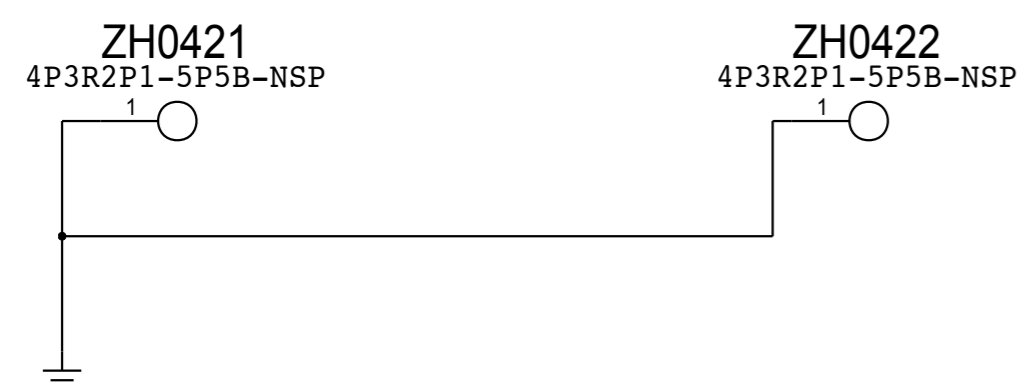
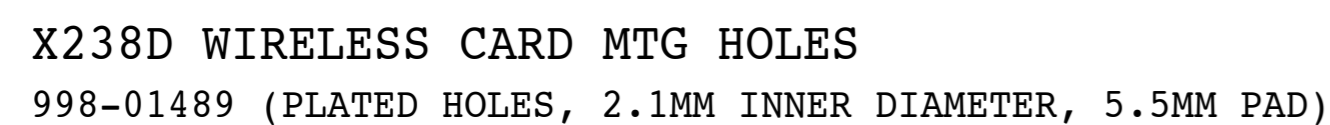
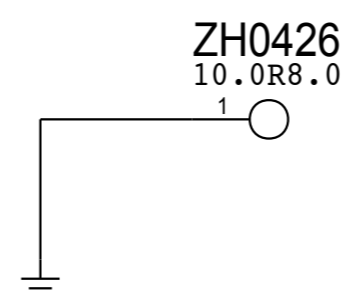
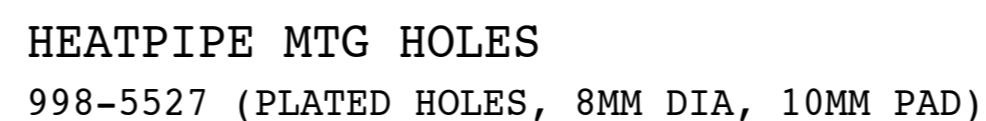
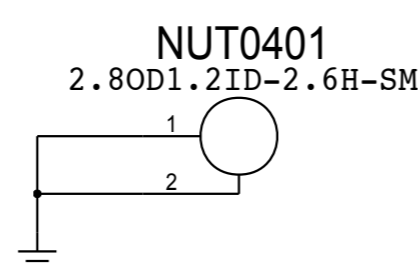
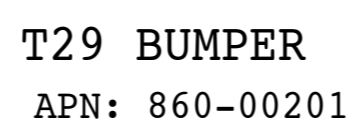
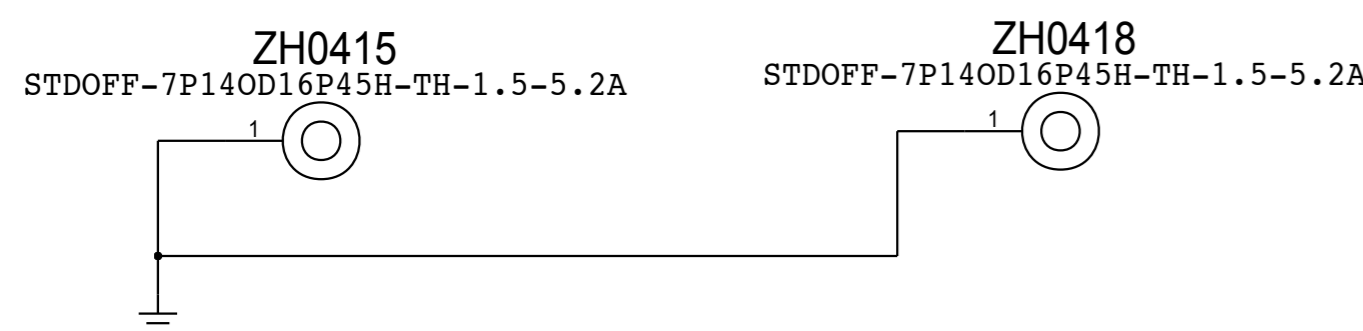
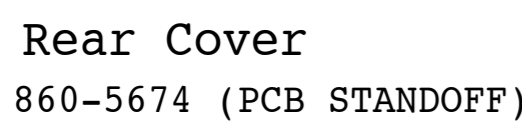
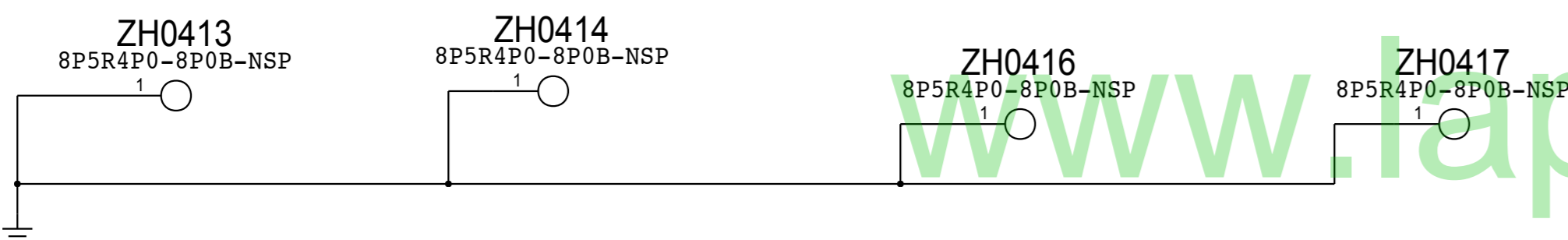
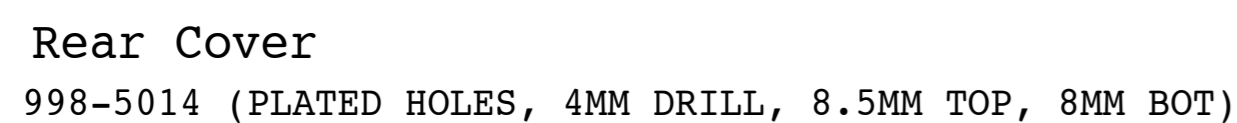
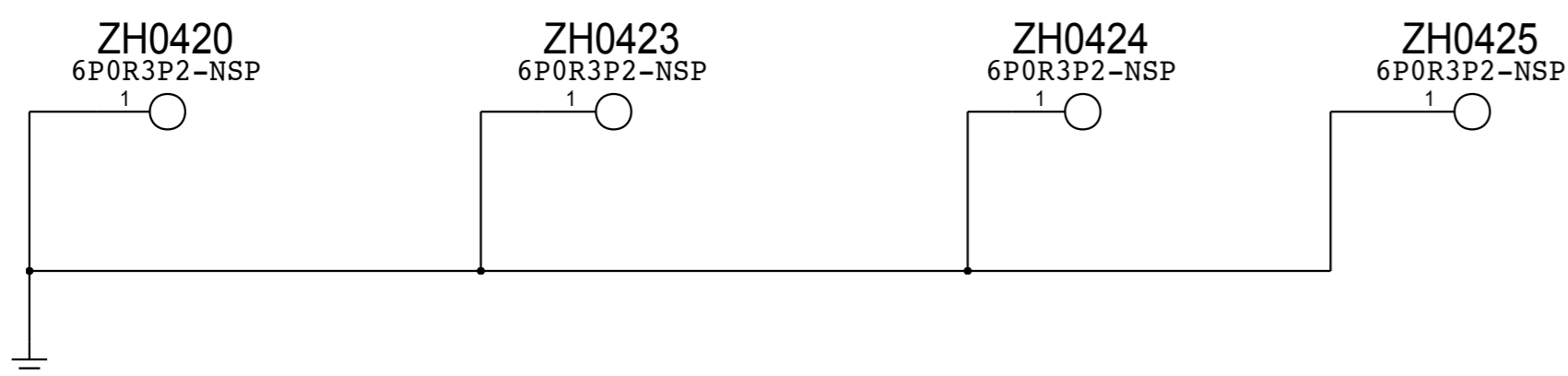
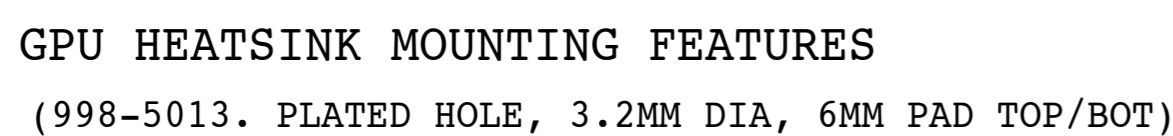
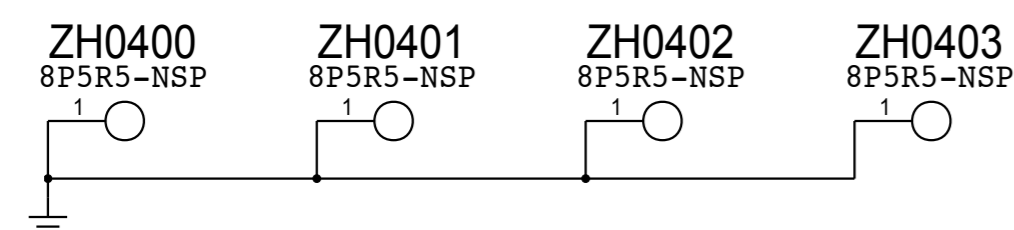
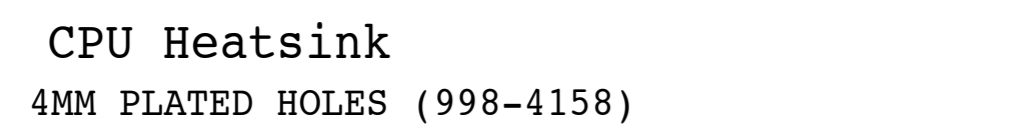


CPUVCC_S0_PWRGD Led



VCCIO_S0_PWRGD Led





EMERALD EMI FENCE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
860-02579	1	FENCE,GPU,EMERALD,90,J95	SF0404	CRITICAL	GPU_Emerald

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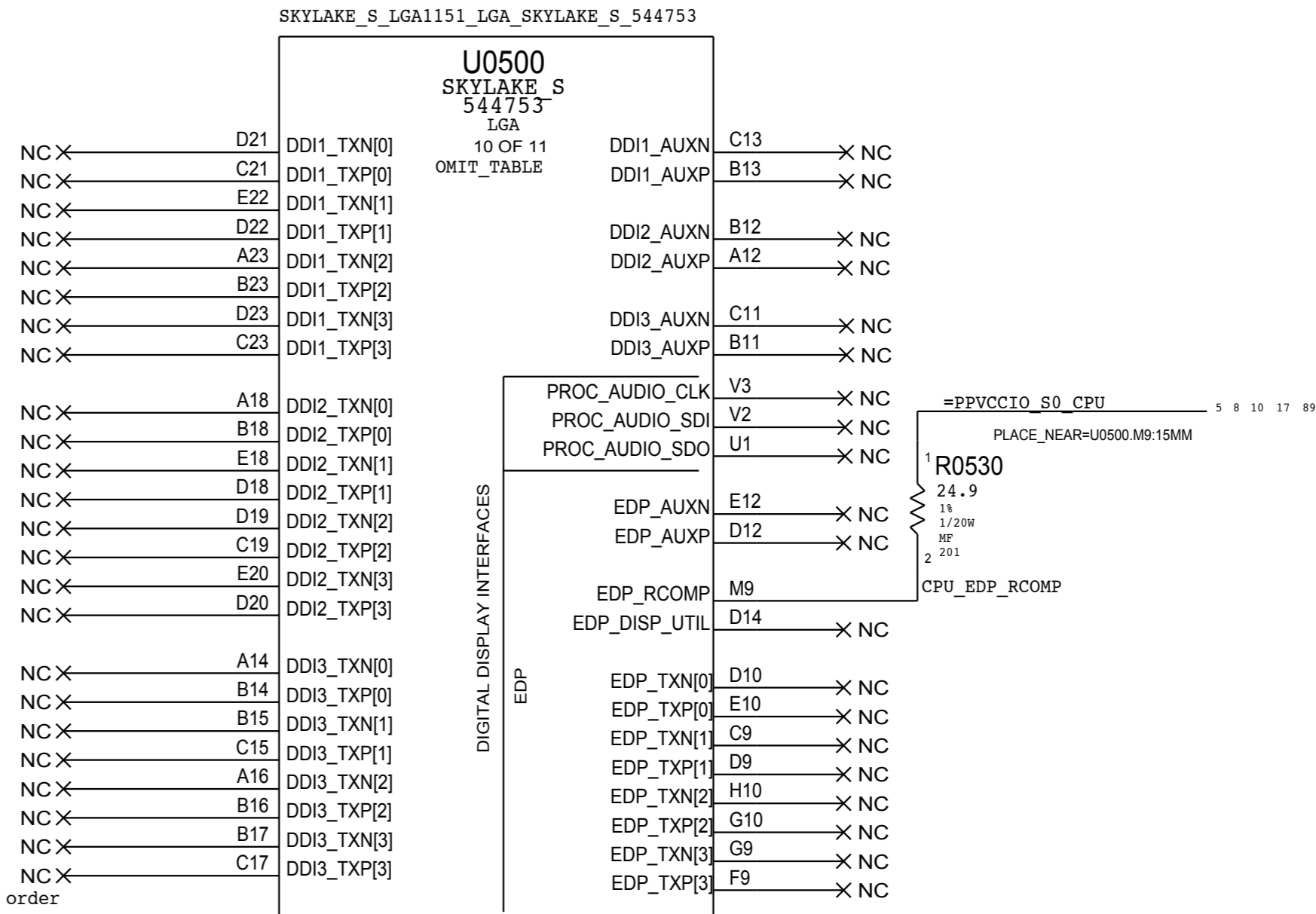
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Port D pins out of order
to match Intel symbol.



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SYNC_MASTER=J78_MLB		SYNC_DATE=06/30/2014	
PAGE TITLE			
CPU & CHIPSET: CPU DMI/PEG/FDI/RSVD			
	Apple Inc.	DRAWING NUMBER	SIZE
		051-00673	D
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		BRANCH	
		PAGE	5 OF 121
		SHEET	5 OF 93

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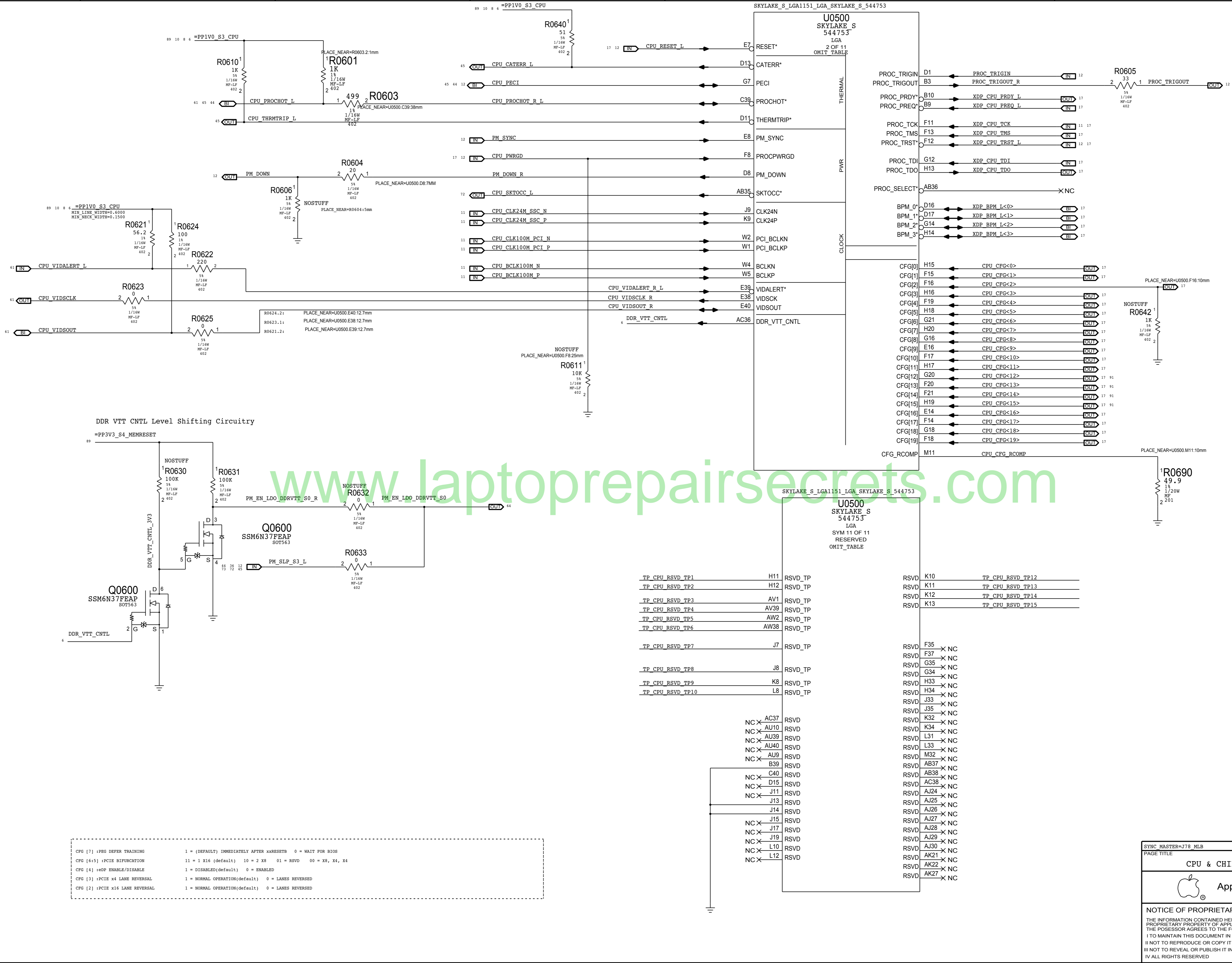
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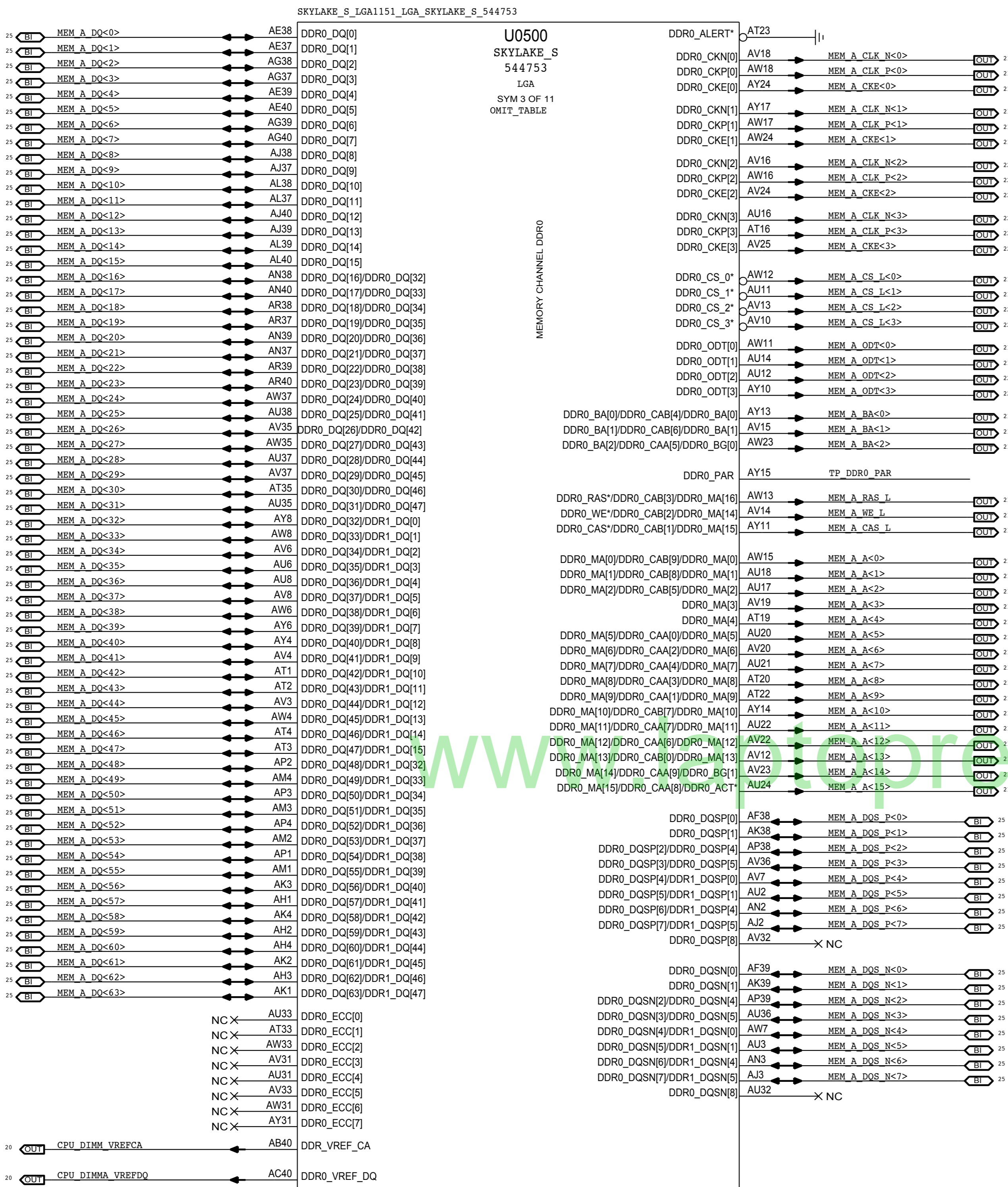
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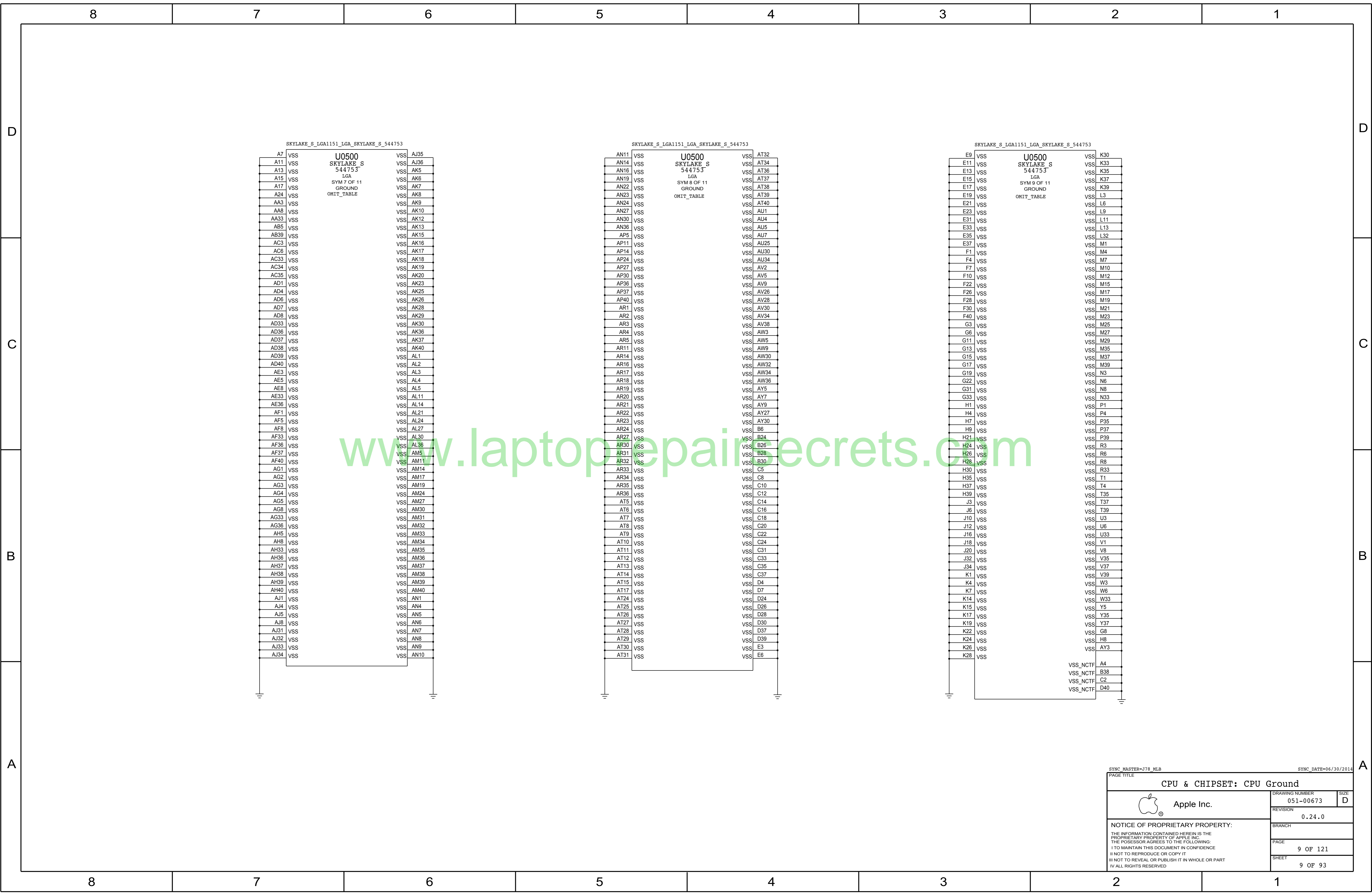
D

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Schematic diagram of the PPVDDO_S3_CPU power plane. The diagram shows a network of capacitors connected to a common rail. The capacitors are:

- C1050, C1051, C1052, C1053, C1054, C1055, C1056, C1057, C1058: 22uF, 20%, 4V, X6S, 0603-1, CRITICAL
- C1040, C1041, C1042: 22uF, 20%, 4V, X6S, 0603-1, NOSTUFF, CRITICAL
- C1099: 4700uF, 0.006OHM, 20%, 2V, POLY, CASE-D2-SM, CRITICAL

1. =PPVCCGT S0 CPU

CRITICAL C1060 22UF 20% 4V X6S 0603-1

CRITICAL C1061 22UF 20% 4V X6S 0603-1

CRITICAL C1062 22UF 20% 4V X6S 0603-1

CRITICAL C1063 22UF 20% 4V X6S 0603-1

CRITICAL C1064 22UF 20% 4V X6S 0603-1

CRITICAL C1065 22UF 20% 4V X6S 0603-1

CRITICAL C1066 22UF 20% 4V X6S 0603-1

CRITICAL C1067 22UF 20% 4V X6S 0603-1

CRITICAL C1068 22UF 20% 4V X6S 0603-1

CRITICAL C1069 22UF 20% 4V X6S 0603-1

CRITICAL C1070 22UF 20% 4V X6S 0603-1

CRITICAL C1071 22UF 20% 4V X6S 0603-1

CRITICAL C1072 22UF 20% 4V X6S 0603-1

CRITICAL C1073 22UF 20% 4V X6S 0603-1

CRITICAL C1074 22UF 20% 4V X6S 0603-1

CRITICAL C1075 22UF 20% 4V X6S 0603-1

CRITICAL C1076 22UF 20% 4V X6S 0603-1

CRITICAL C1077 22UF 20% 4V X6S 0603-1

CRITICAL C1078 22UF 20% 4V X6S 0603-1

CRITICAL C1079 22UF 20% 4V X6S 0603-1

CRITICAL C1080 22UF 20% 4V X6S 0603-1

CRITICAL C1081 22UF 20% 4V X6S 0603-1

CRITICAL C1082 22UF 20% 4V X6S 0603-1

CRITICAL C1083 22UF 20% 4V X6S 0603-1

CRITICAL C1084 22UF 20% 4V X6S 0603-1

CRITICAL C1085 22UF 20% 4V X6S 0603-1

CRITICAL C1086 22UF 20% 4V X6S 0603-1

CRITICAL C1087 22UF 20% 4V X6S 0603-1

CRITICAL C1088 22UF 20% 4V X6S 0603-1

CRITICAL C1089 22UF 20% 4V X6S 0603-1

89 8 =PPVCCSA S0_CPU

1 C10C0 220UF 20V X6S 0603-1
 2

1 C10C1 CRITICAL 220UF 20V X6S 0603-1
 2

1 C10C2 CRITICAL 220UF 20V X6S 0603-1
 2

1 C10C3 CRITICAL 220UF 20V X6S 0603-1
 2

1 C10C4 1.00UF 10V X6S 0402
 2

1 C10C7 1.00UF 10V X6S 0402
 2

89 8 6 =PP1V0_S3_CPU


1 C10C9 220UF 20V X6S 0603-1
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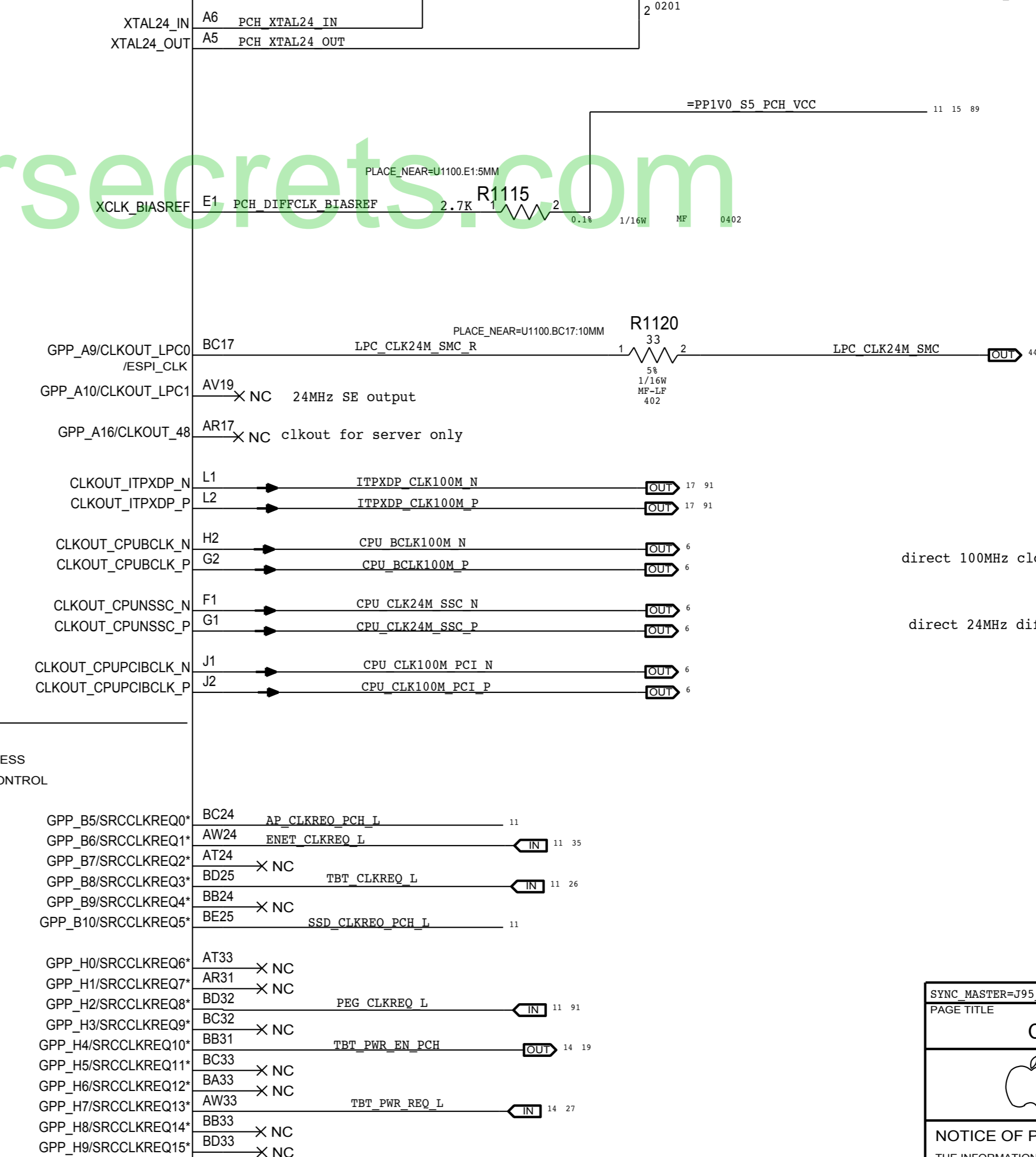
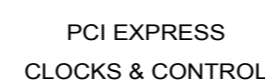
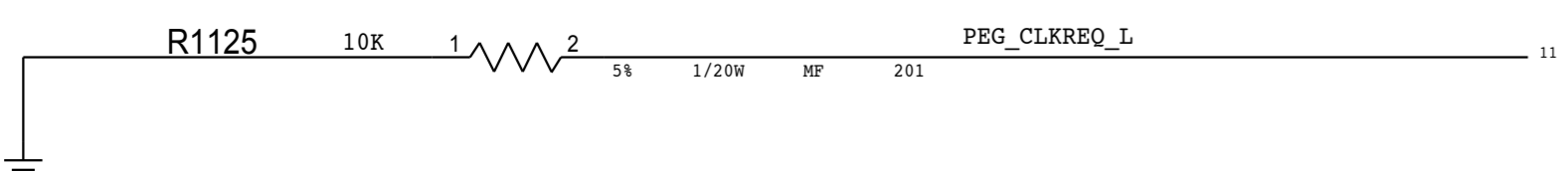
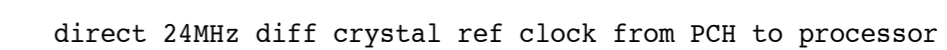
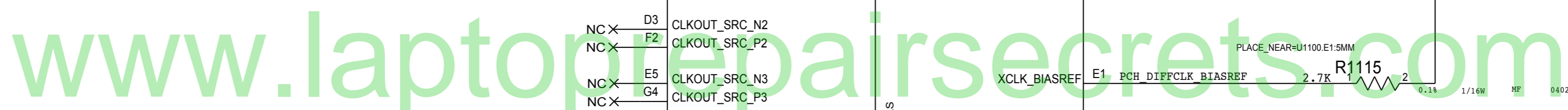
1 C10C5 220UF 20V X6S 0603-1
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1 C10C6 1.00UF 10V X6S 0402
 2

1 C10C8 1.00UF 10V X6S 0402
 2

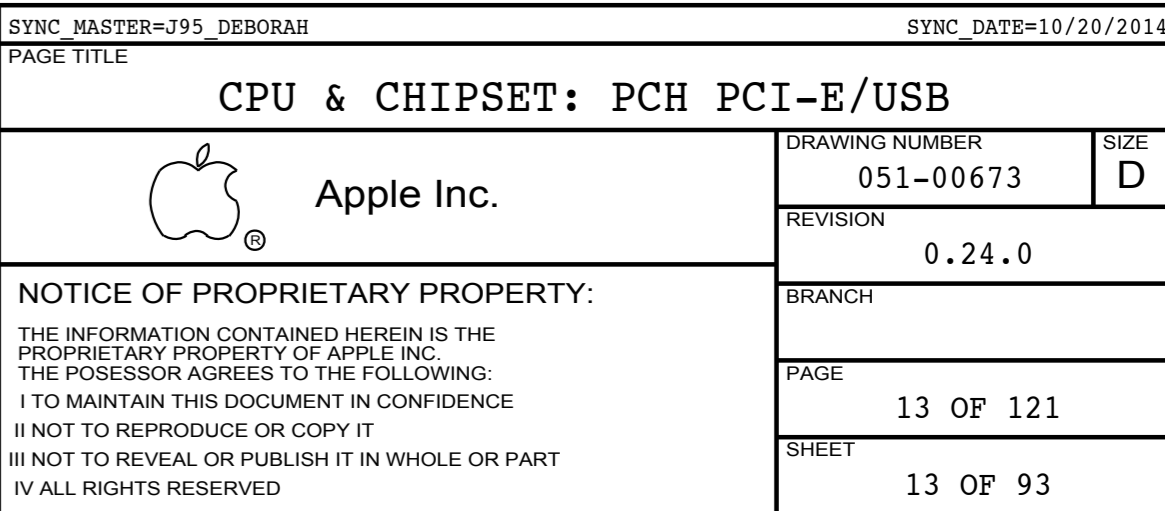
1 C10B6 CRITICAL 470UF-0.0060HM 20V POLY C95E-D2-SM
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SYNC MASTER=J78 MLB		SYNC DATE=06/30/2014	
PAGE TITLE			
CPU & CHIPSET: CPU Decoupling			
 Apple Inc.		DRAWING NUMBER	SIZE
		051-00673	D
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		BRANCH	
		PAGE	10 OF 121
		SHEET	10 OF 93



SYNC MASTER=J95 DEBORAH	SYNC DATE=10/20/2014	
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	BRANCH	PAGE <div style="display: flex; justify-content: space-between; font-weight: bold;"> 11 OF 121 </div>
SHEET <div style="display: flex; justify-content: space-between; font-weight: bold;"> 11 OF 93 </div>		





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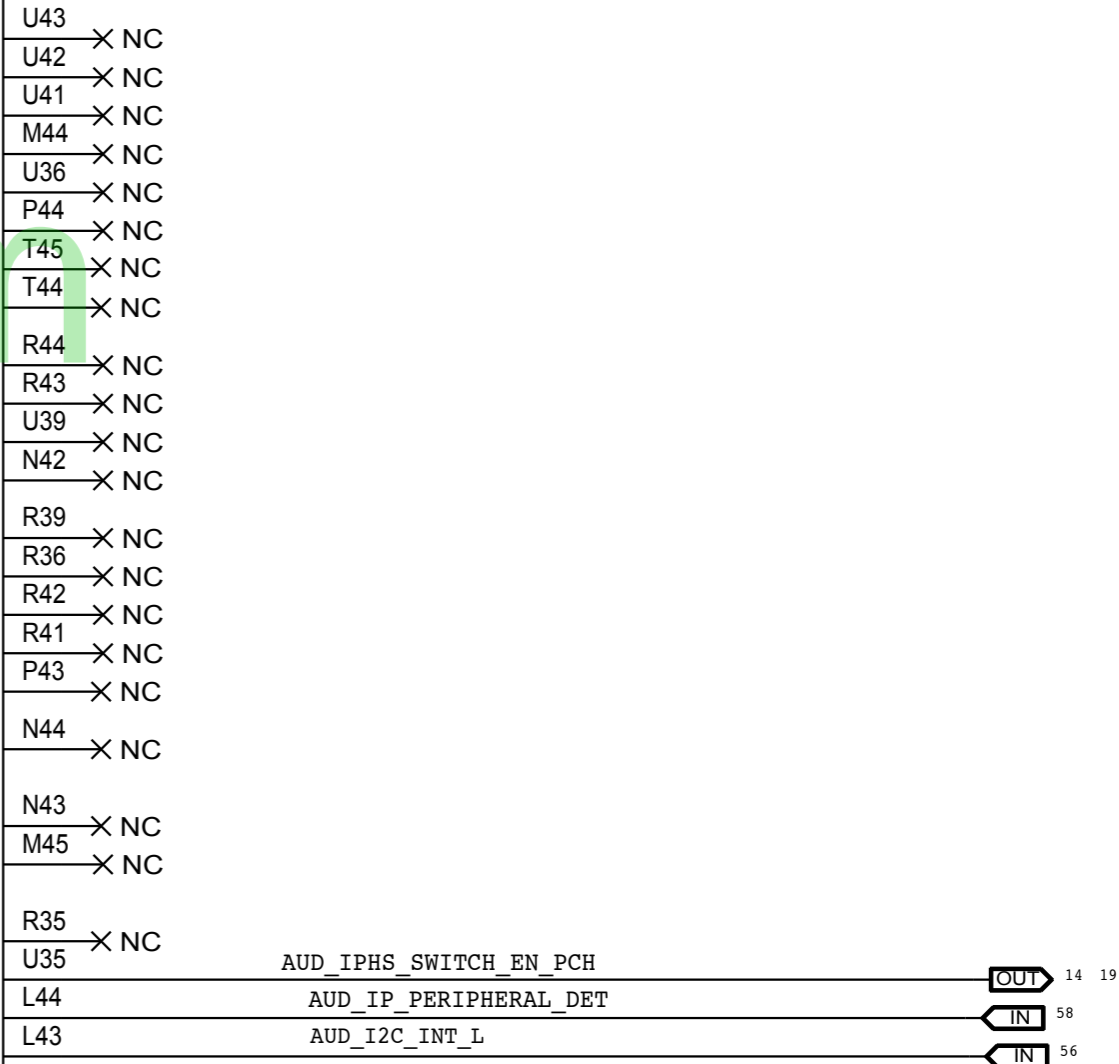
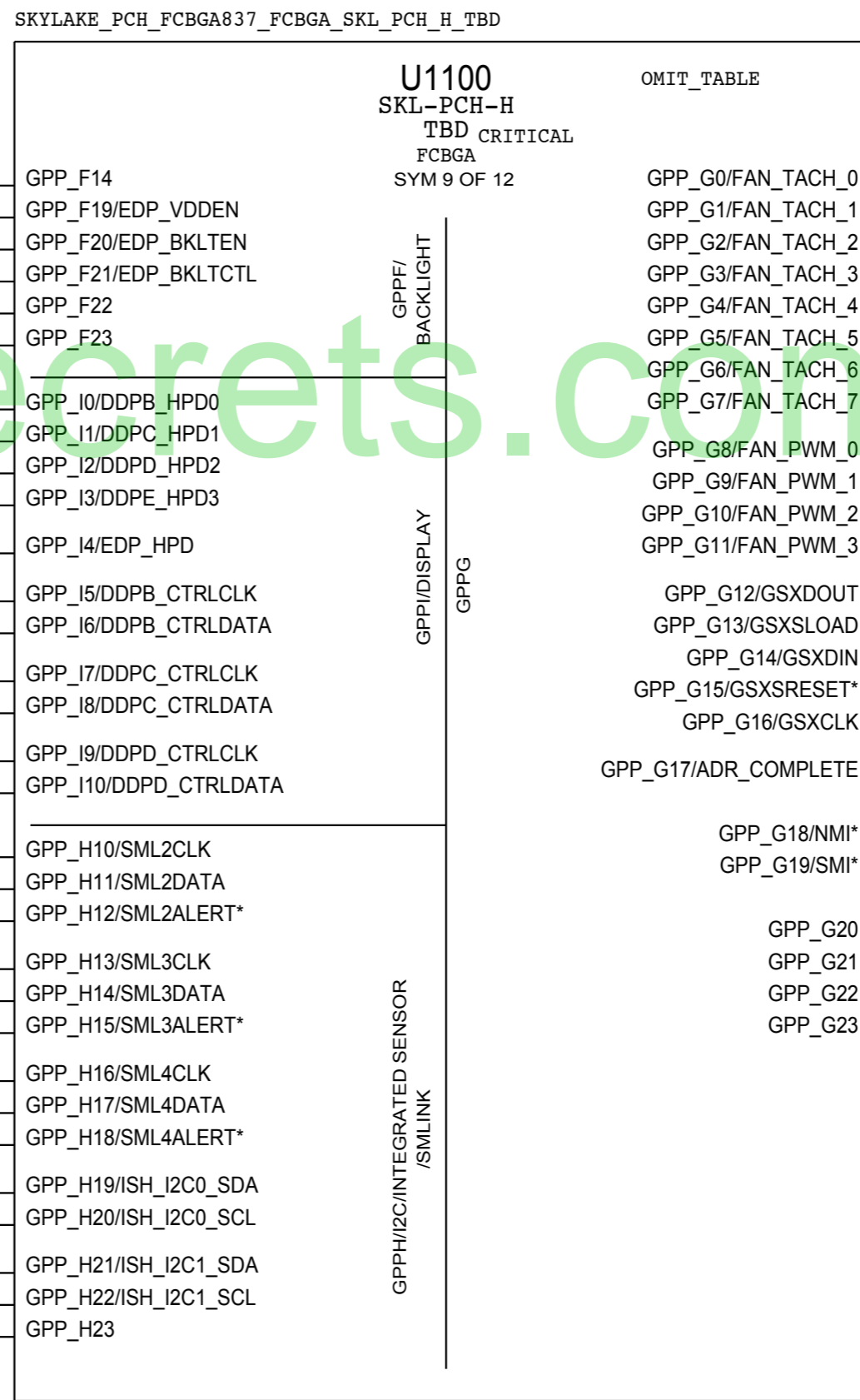
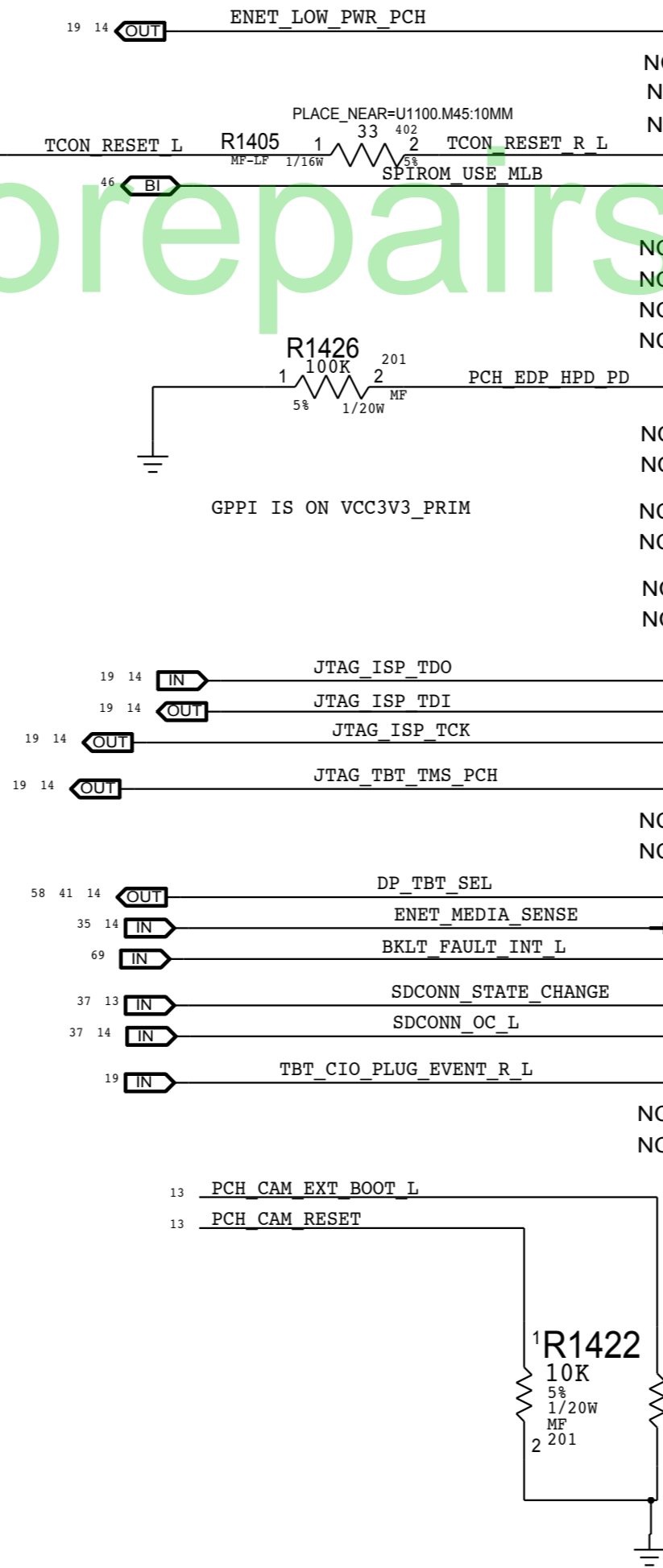
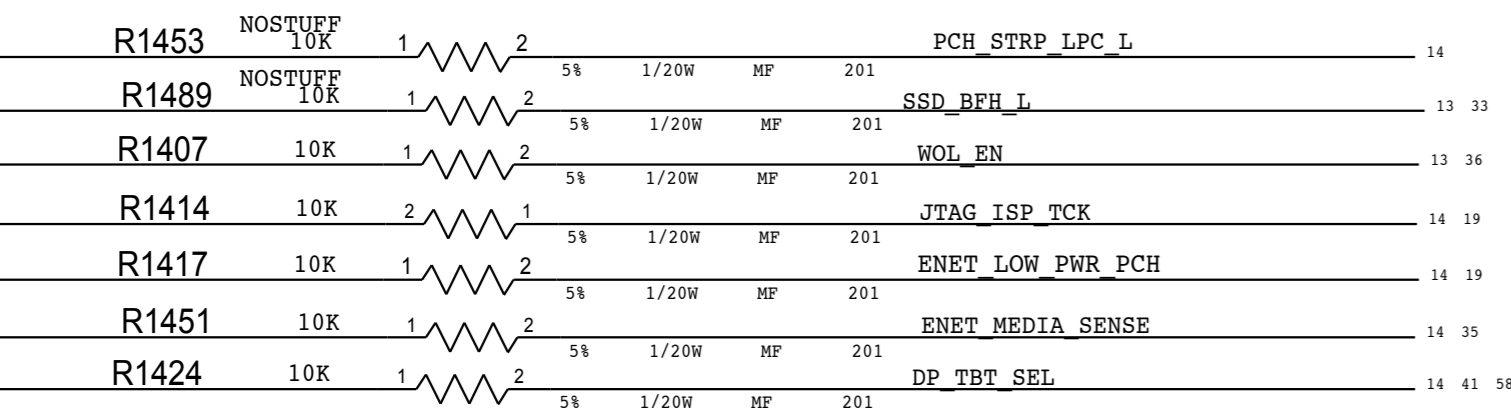
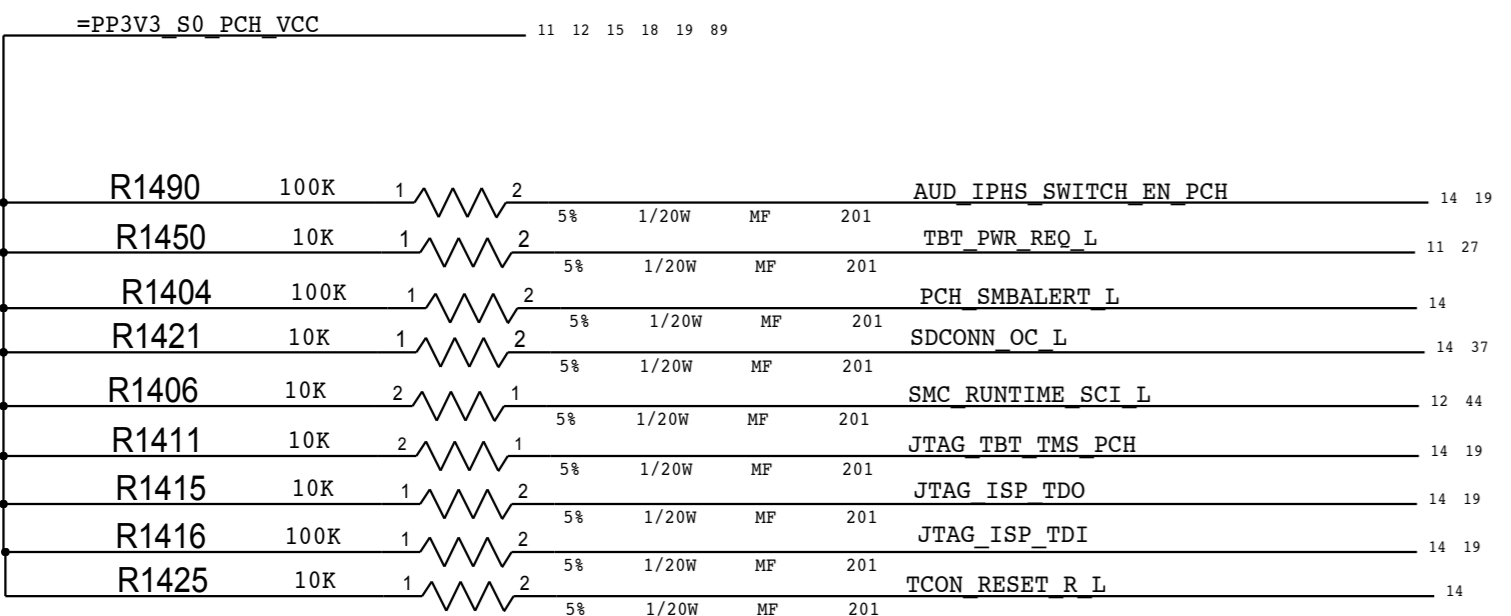
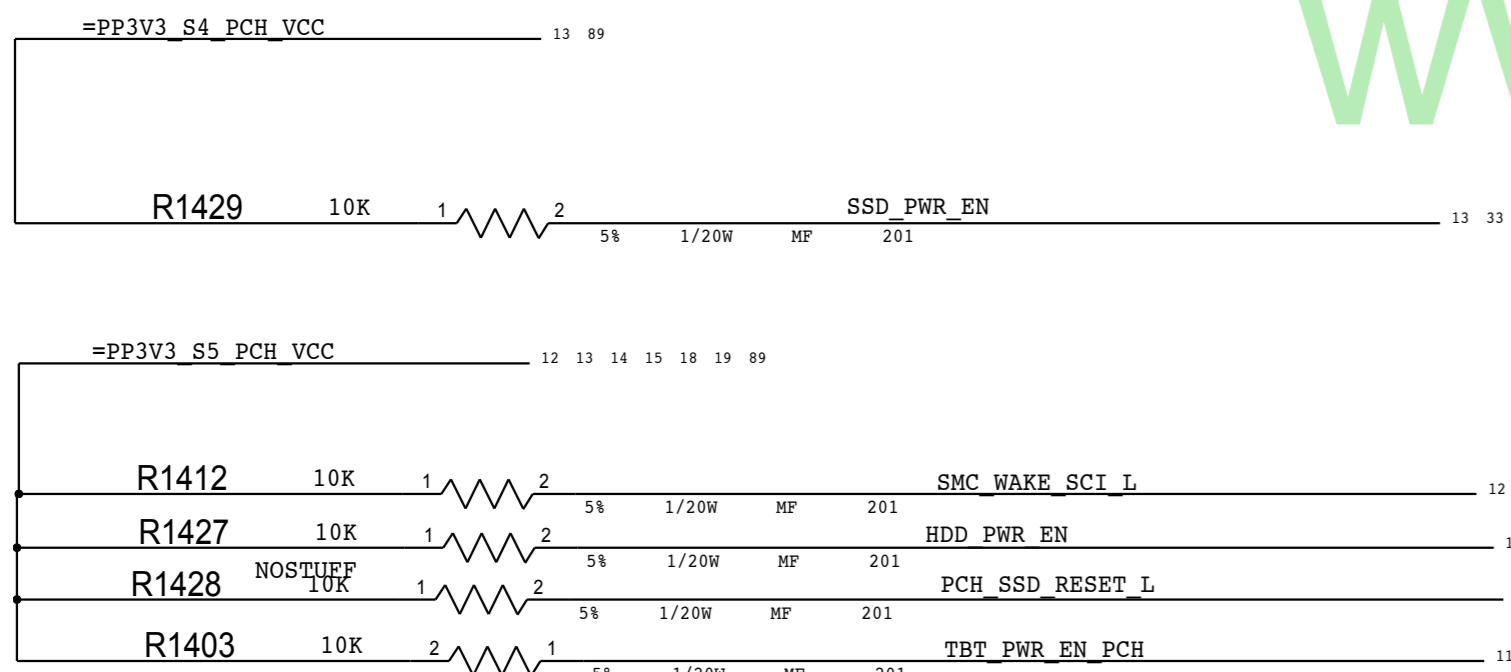
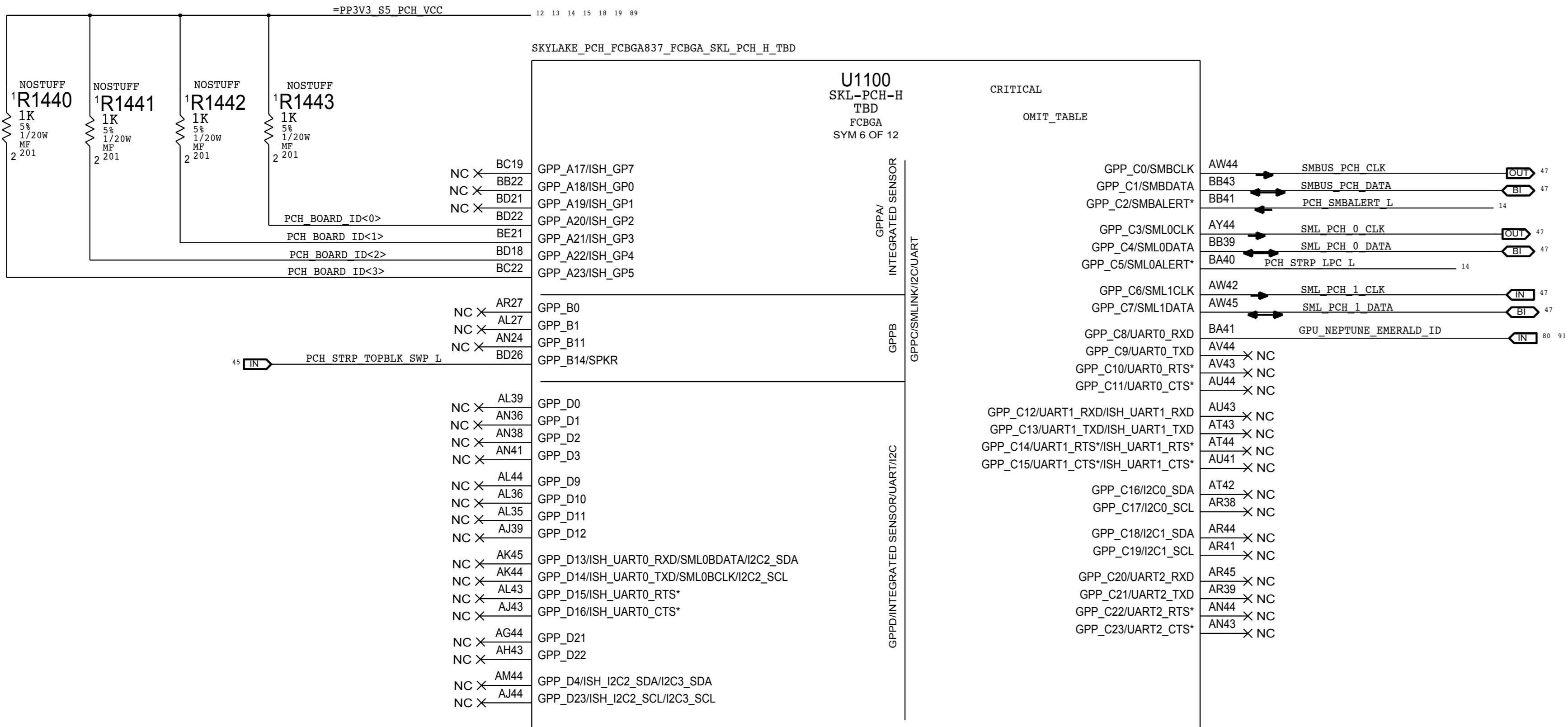
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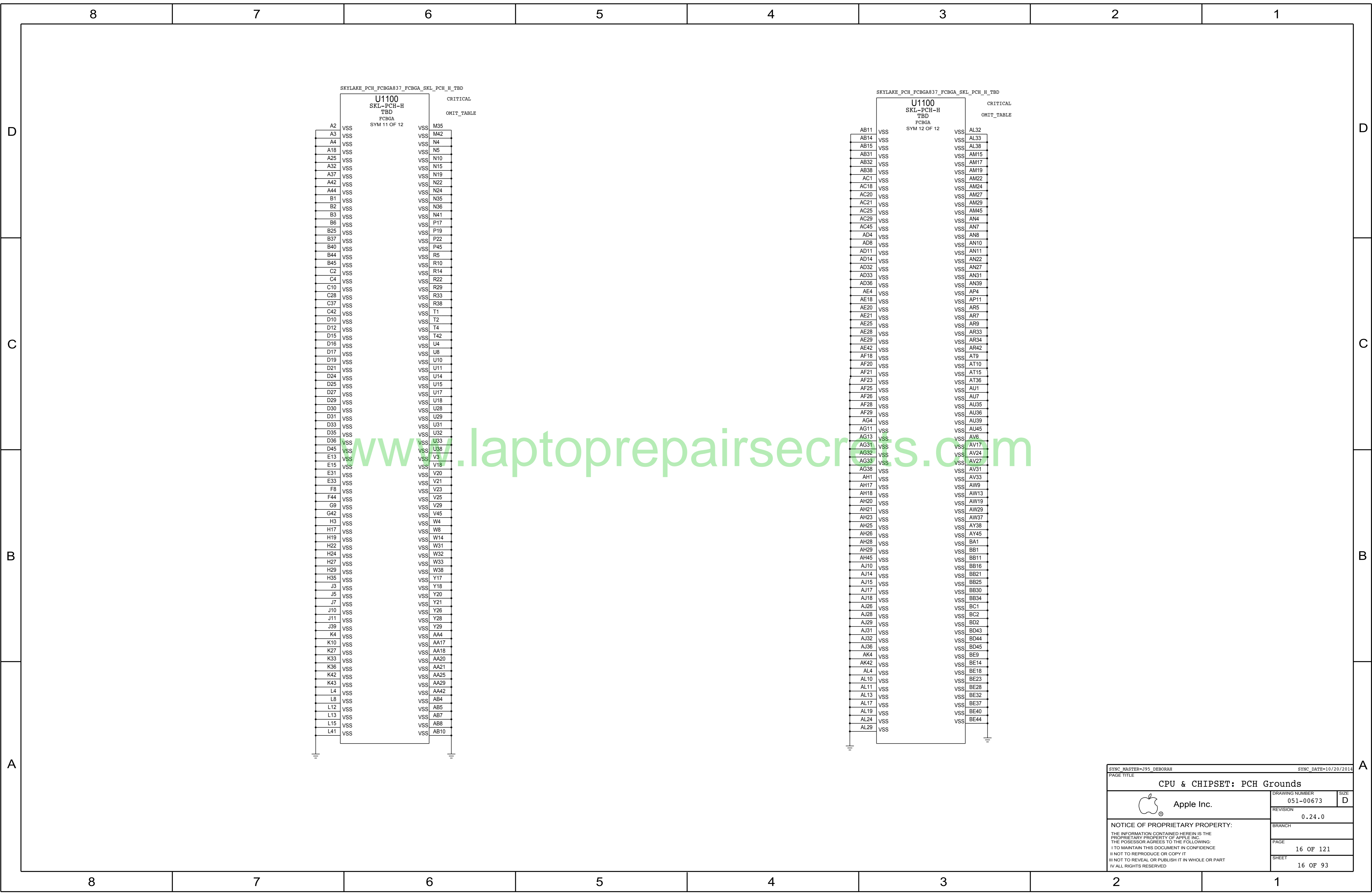
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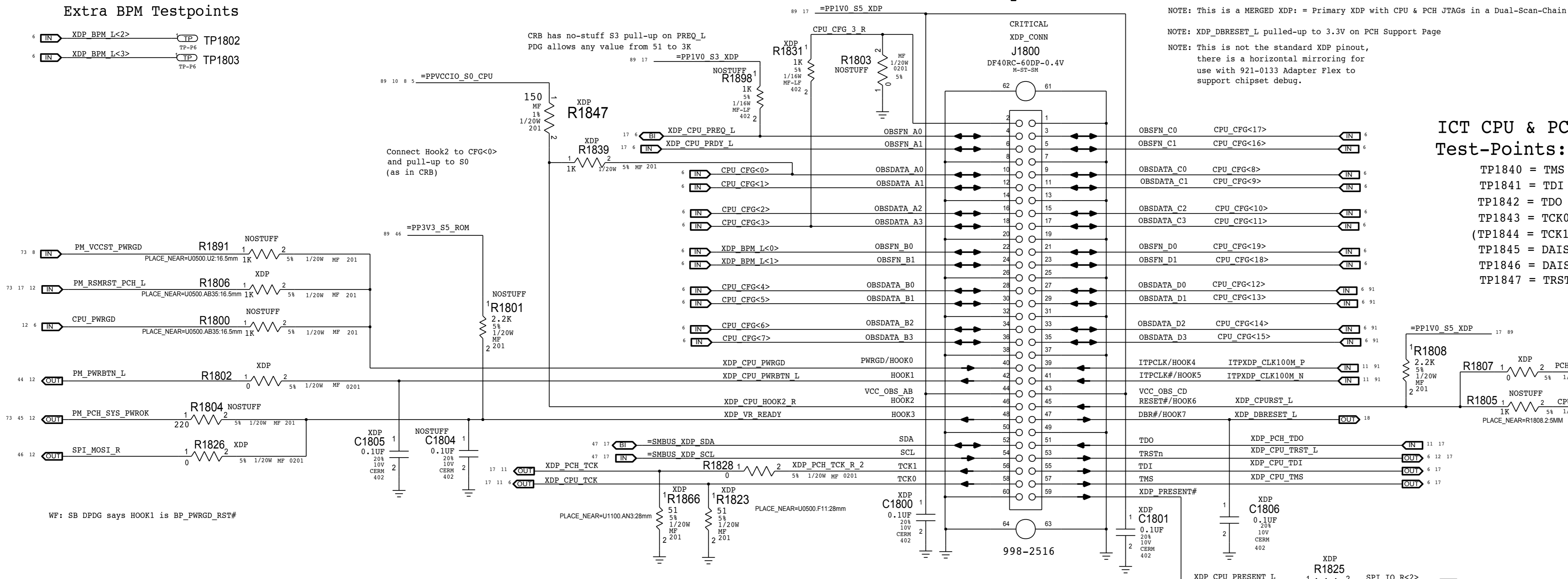
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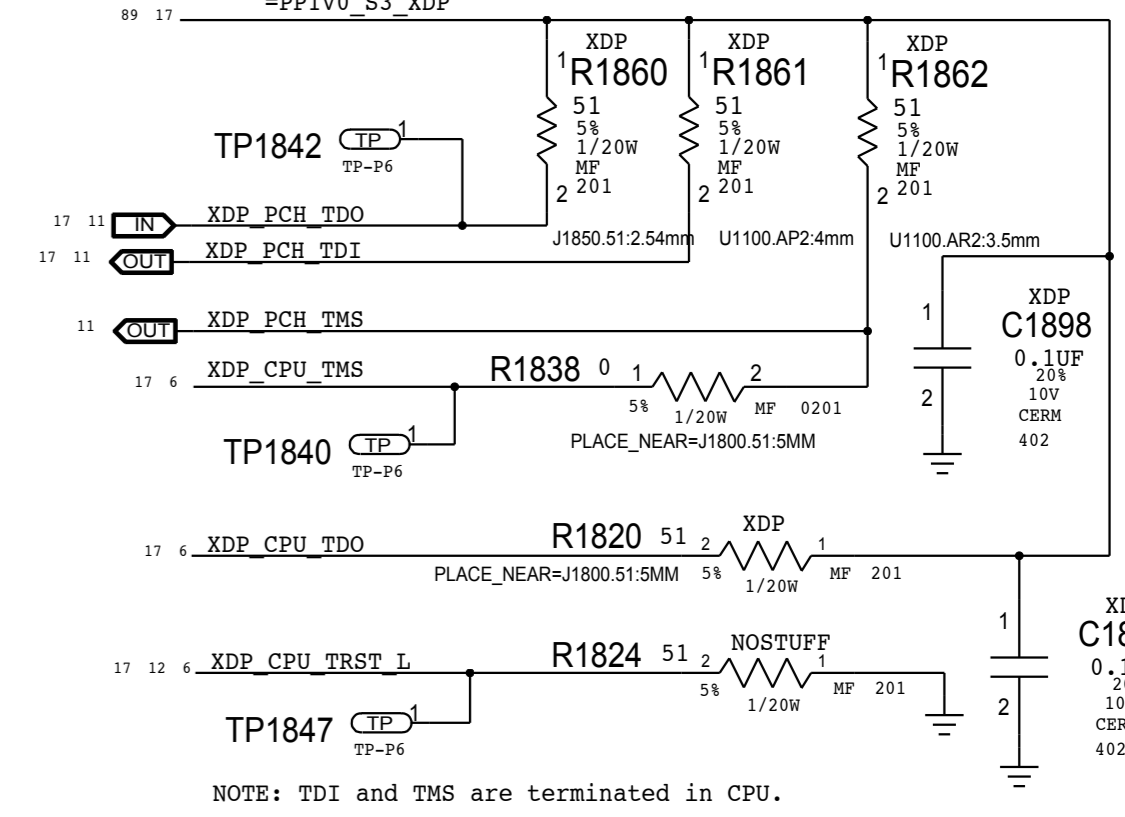
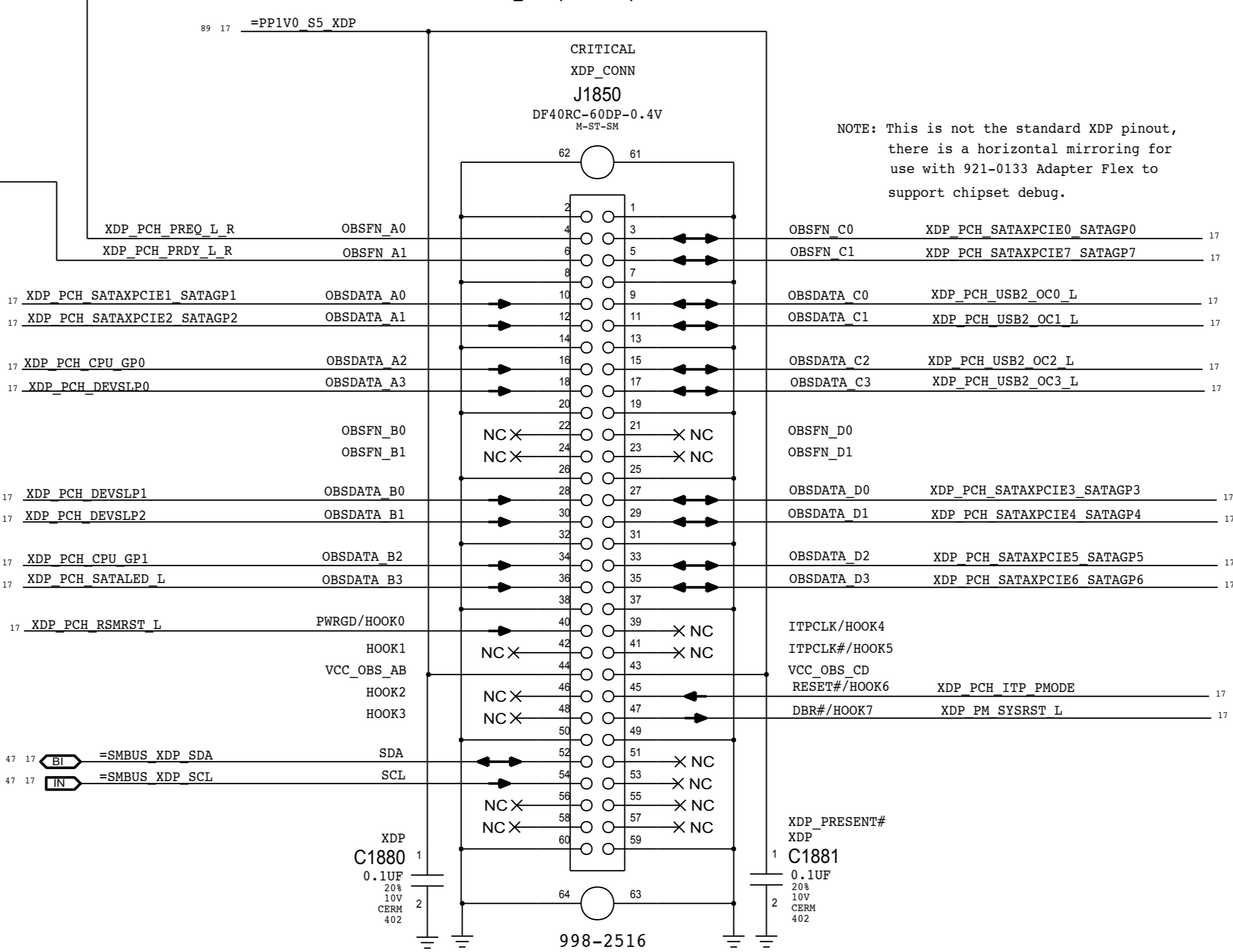
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Primary Micro2-XDP

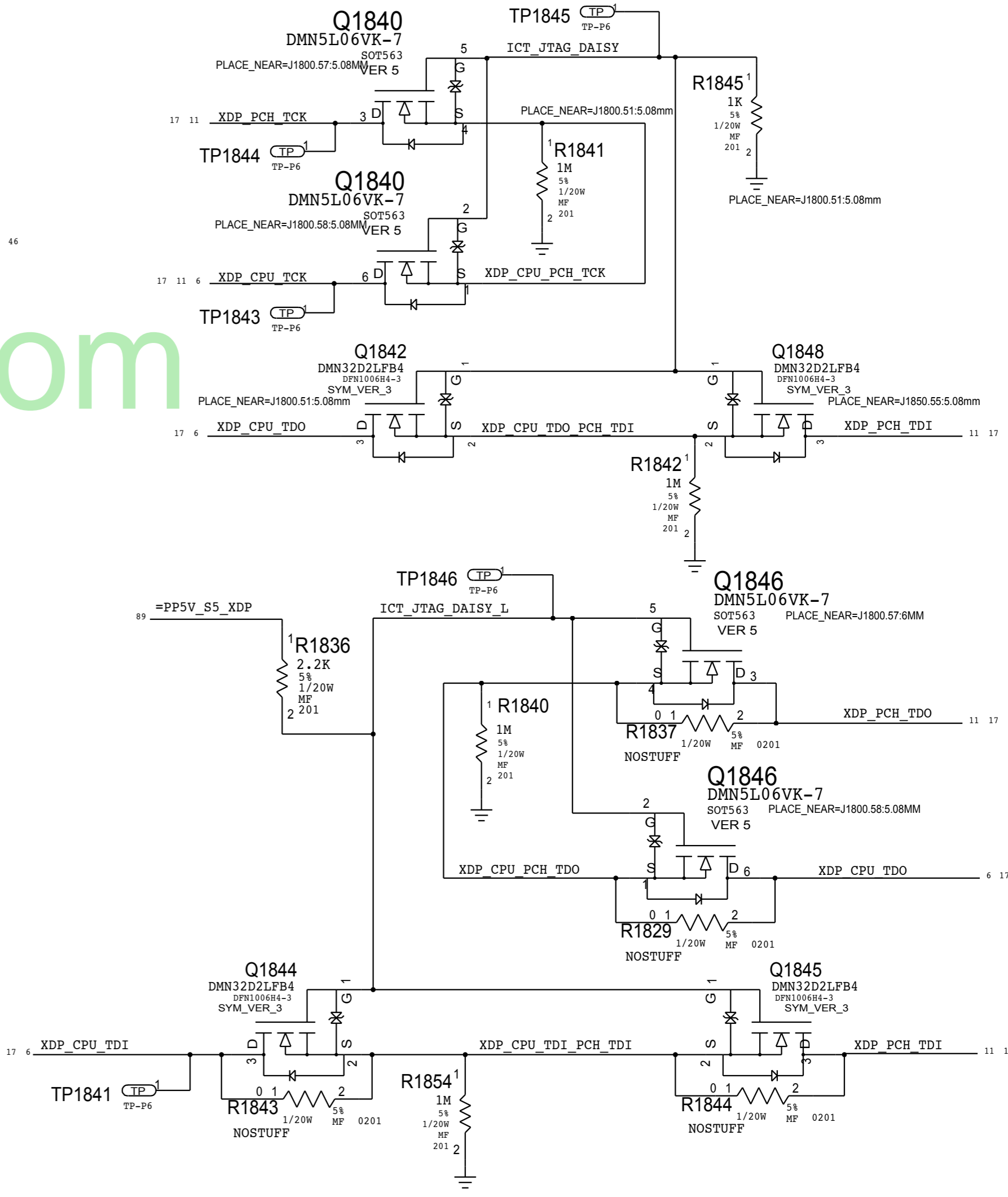


Secondary (PCH) Micro2-XDP



ICT CPU & PCH JTAG Daisy-Chain Support (S0):


To configure CPU and PCH JTAG in an ICT Daisy-Chain:
Drive ICT_JTAG_DAISY to 5V and drive ICT_JTAG_DAISY_L to Ground.



PCH SIGNALS				XDP SIGNALS			
IN	PCH_PREQ_L	OMIT R1890	SHORT	1	2	XDP_PCH_PREQ_L	17
IN	PCH_PRDY_L	OMIT R1893	SHORT	1	2	XDP_PCH_PRDY_L	17
BI	PCH_SATAXPIC10 SATAGP0	OMIT R1894	SHORT	1	2	XDP_PCH_SATAXPIC10 SATAGP0	17
BI	PCH_SATAXPIC11 SATAGP1	OMIT R1895	SHORT	1	2	XDP_PCH_SATAXPIC11 SATAGP1	17
BI	PCH_SATAXPIC12 SATAGP2	OMIT R1880	SHORT	1	2	XDP_PCH_SATAXPIC12 SATAGP2	17
BI	PCH_SATAXPIC13 SATAGP3	OMIT R1881	SHORT	1	2	XDP_PCH_SATAXPIC13 SATAGP3	17
BI	PCH_SATAXPIC14 SATAGP4	OMIT R1896	SHORT	1	2	XDP_PCH_SATAXPIC14 SATAGP4	17
BI	PCH_SATAXPIC15 SATAGP5	OMIT R1897	SHORT	1	2	XDP_PCH_SATAXPIC15 SATAGP5	17
BI	PCH_SATAXPIC16 SATAGP6	OMIT R1872	SHORT	1	2	XDP_PCH_SATAXPIC16 SATAGP6	17
BI	PCH_SATAXPIC17 SATAGP7	OMIT R1873	SHORT	1	2	XDP_PCH_SATAXPIC17 SATAGP7	17
BI	XDP_PCH_OBSDATA_A2	OMIT R1874	SHORT	1	2	XDP_PCH_CPU_GP0	17
BI	PCH_DEVSLP0	OMIT R1875	SHORT	1	2	XDP_PCH_DEVSLP0	17
BI	PCH_ITP_PMODE	OMIT R1878	SHORT	1	2	XDP_PCH_ITP_PMODE	17
BI	PCH_DEVSLP1	OMIT R1879	SHORT	1	2	XDP_PCH_DEVSLP1	17
BI	PCH_DEVSLP2	OMIT R1882	SHORT	1	2	XDP_PCH_DEVSLP2	17
BI	XDP_PCH_OBSDATA_B2	OMIT R1883	SHORT	1	2	XDP_PCH_CPU_GP1	17
BI	PCH_SATALED_L	OMIT R1886	SHORT	1	2	XDP_PCH_SATALED_L	17
BI	PM_RSMRST_PCH_L	OMIT R1887	SHORT	1	2	XDP_PCH_RSMRST_L	17
BI	PM_SYSRST_L	OMIT R1884	SHORT	1	2	XDP_PCH_SYSRST_L	17
BI	USB_EXT_A_OC_L	OMIT R1833	SHORT	1	2	XDP_PCH_USB2_OC0_L	17
BI	USB_EXT_B_OC_L	OMIT R1835	SHORT	1	2	XDP_PCH_USB2_OC1_L	17
BI	USB_EXT_C_OC_L	OMIT R1832	SHORT	1	2	XDP_PCH_USB2_OC2_L	17
BI	USB_EXT_D_OC_L	OMIT R1834	SHORT	1	2	XDP_PCH_USB2_OC3_L	17

PCH/XDP Signal Isolation Notes:

R187x and R189x should be placed where signal path needs to split between route from PCH to J1850 and path to non-XDP signal destination (to minimize stub).

SYNC_MASTER=J95_ANDREW		SYNC_DATE=01/24/2015	
PAGE TITLE			
CPU & CHIPSET: XDP			
 Apple Inc.	DRAWING NUMBER 051-00673		SIZE D
	REVISION 0.24.0		
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		PAGE	18 OF 121
		SHEET	17 OF 93

D

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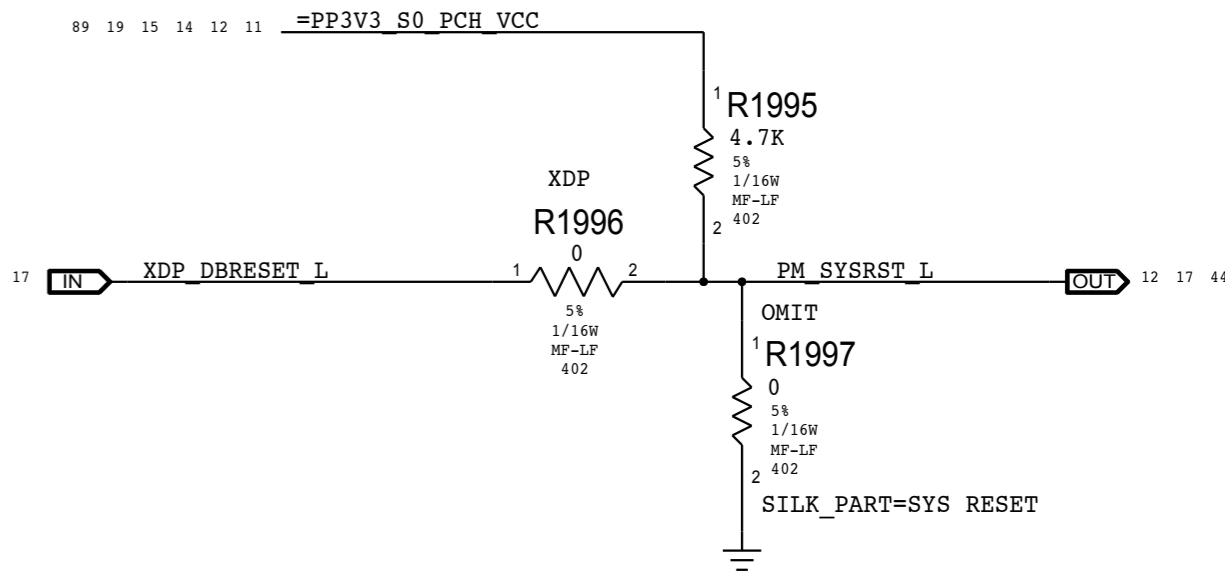
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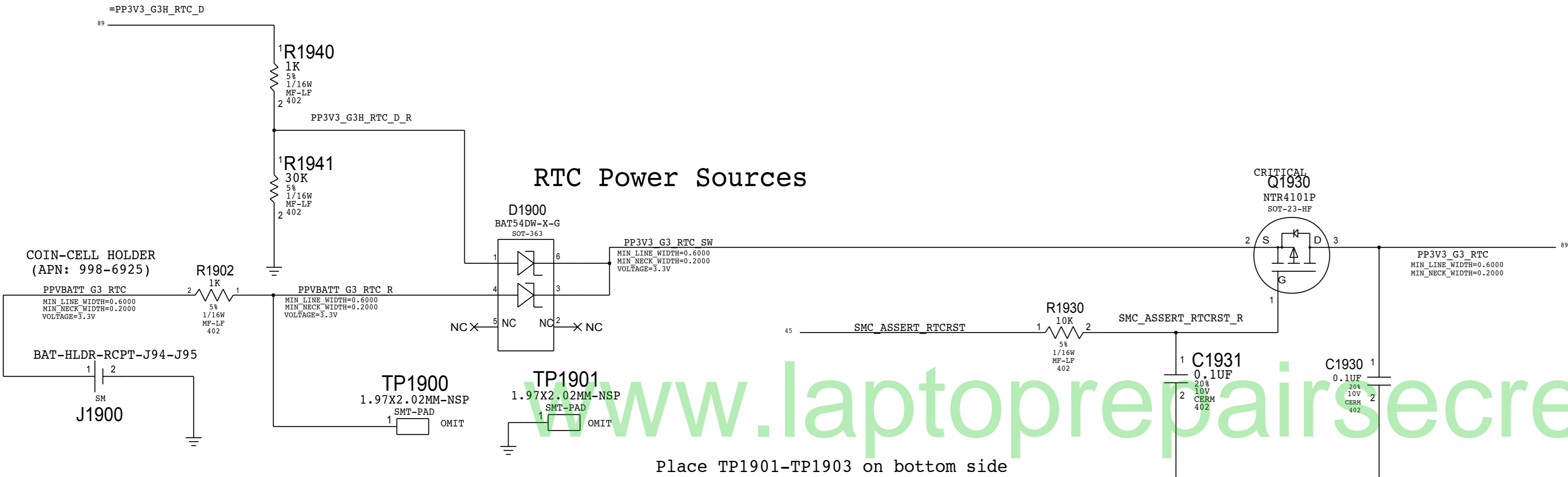
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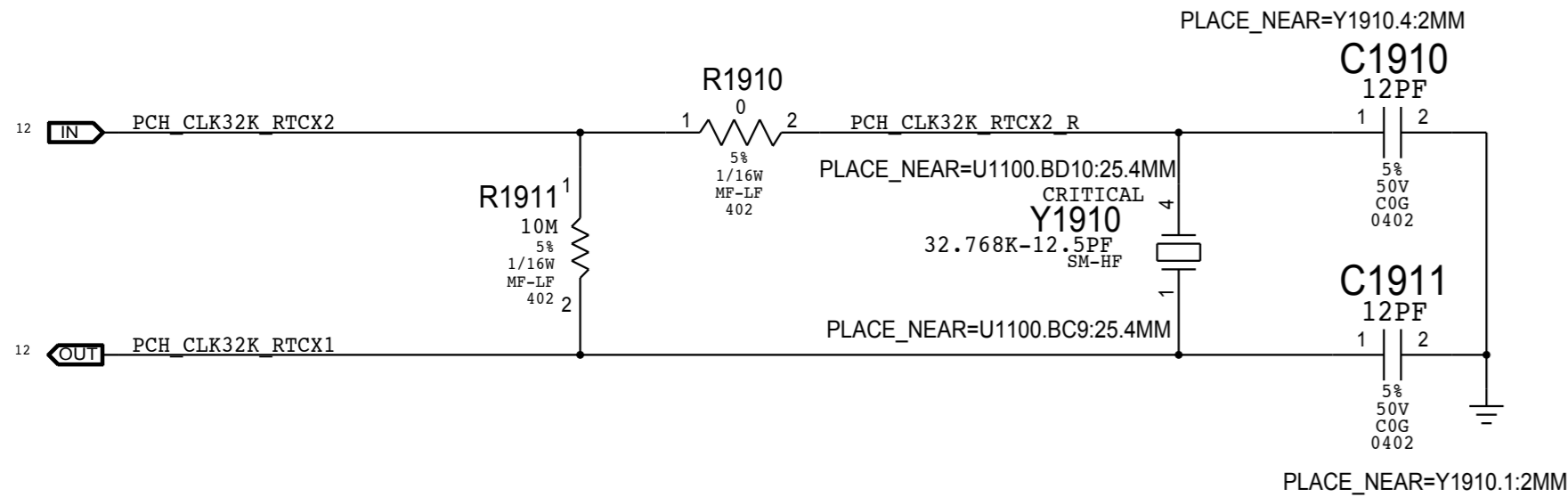
PCH Reset Button



RTC Power Sources

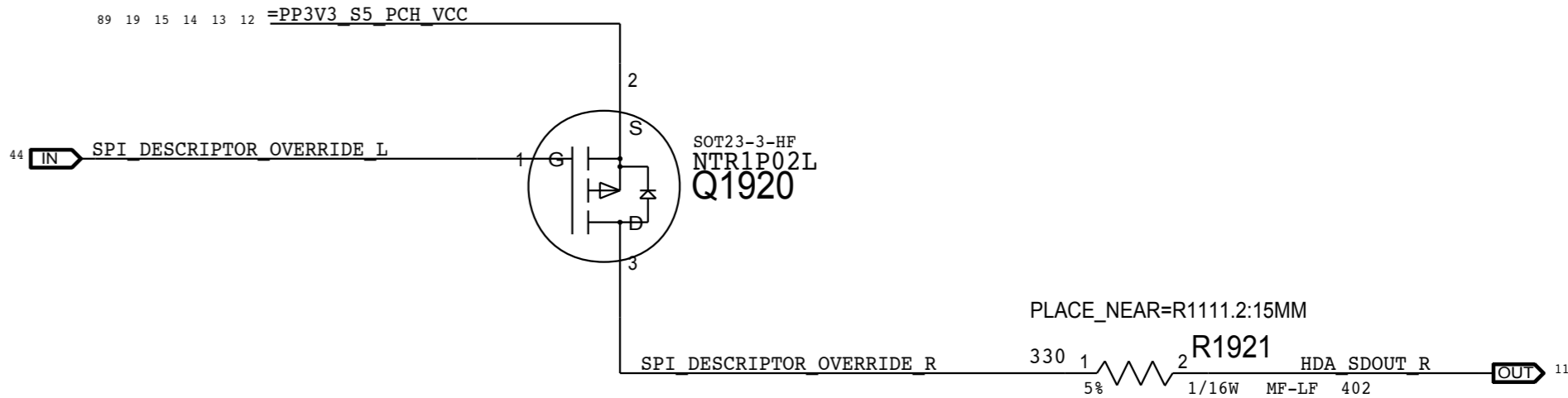


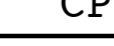
PCH RTC Crystal



PCH ME Disable Strap

PCH uses HDA_SDO as a power-up strap. If low, ME functions normally. If high, ME is disabled. This allows for full re-flashing of SPI ROM. SMC controls strap enable to allow in-field control of strap setting.



SYNC_MASTER=BRANCH_SYEDKAR		SYNC_DATE=09/10/2014	
PAGE TITLE			
CPU & CHIPSET: Chipset Support			
 Apple Inc.	DRAWING NUMBER	051-00673	SIZE
	REVISION	0.24.0	D
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		PAGE	19 OF 121
		SHEET	18 OF 93

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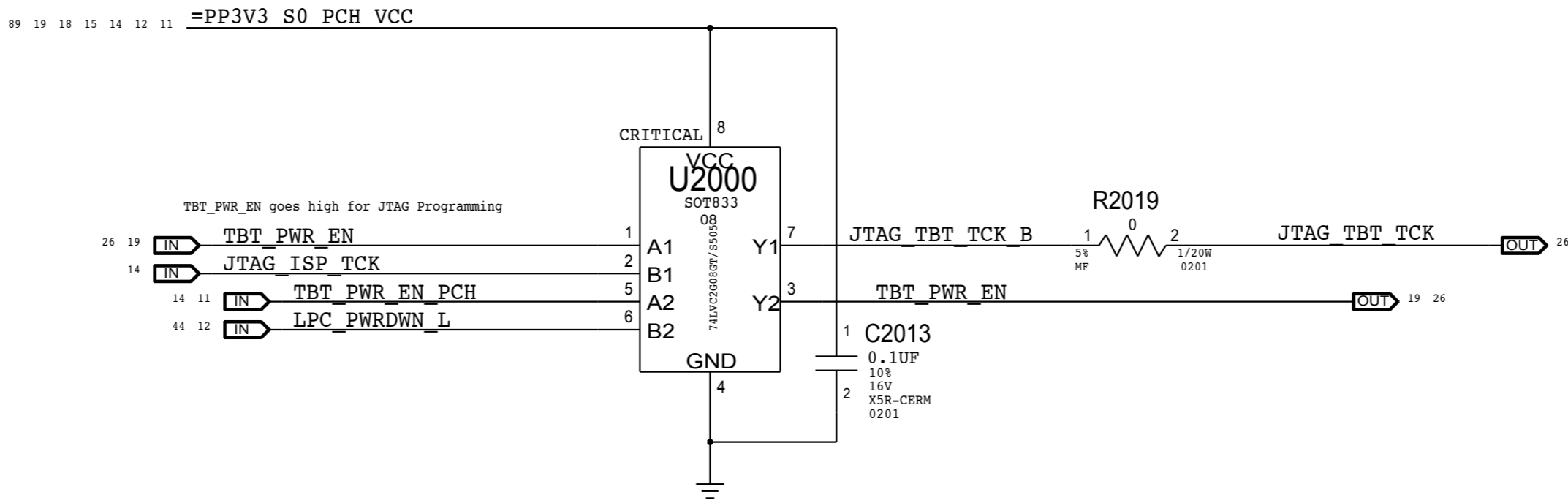
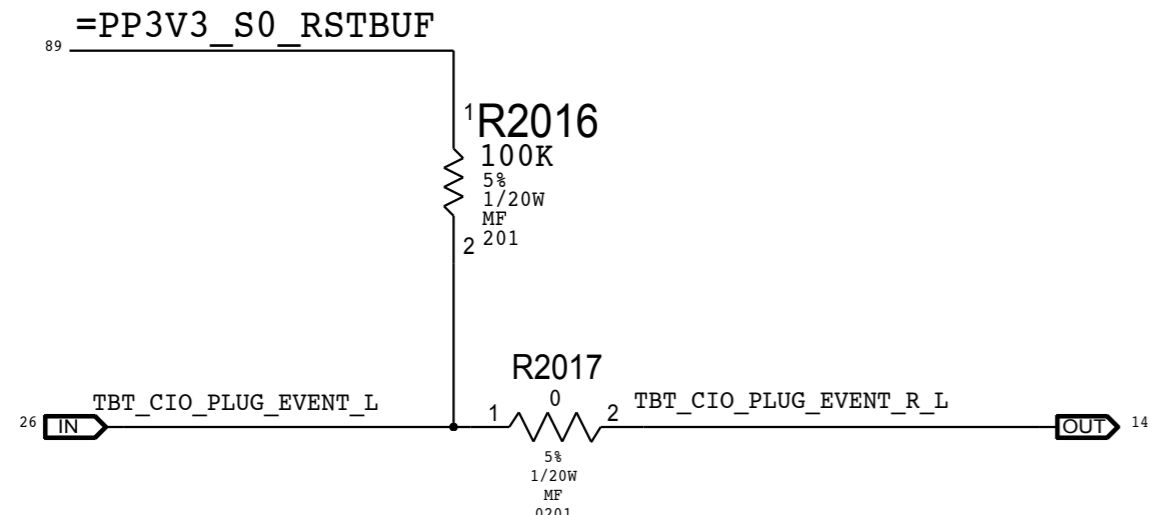
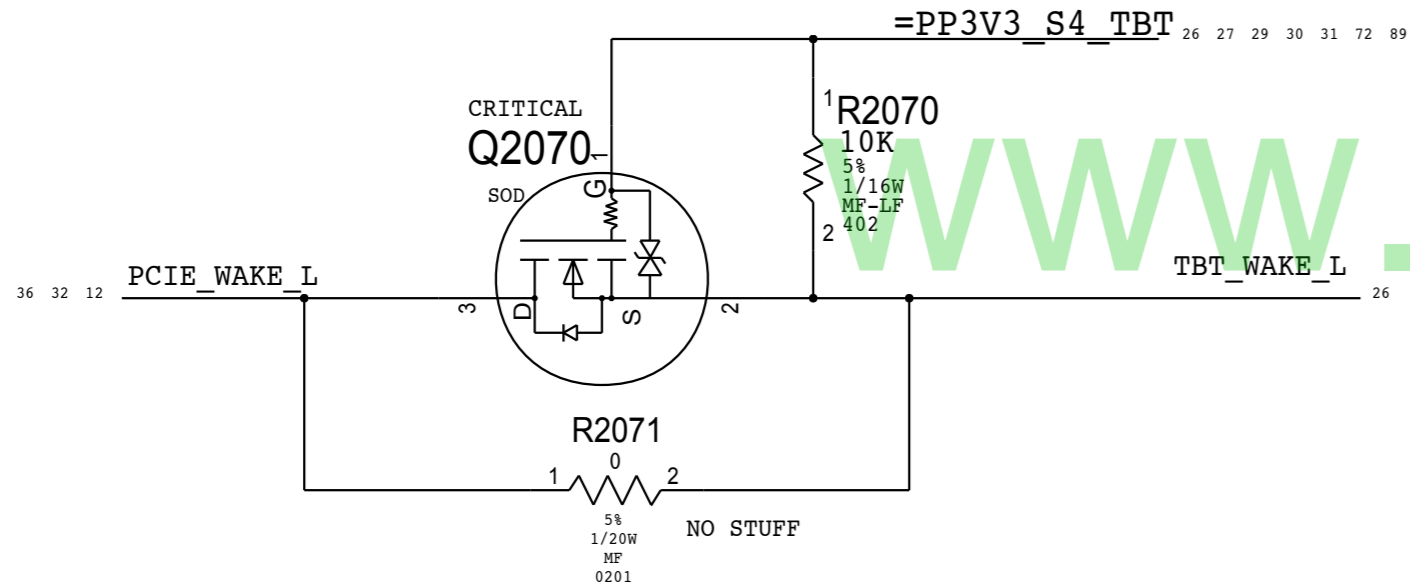
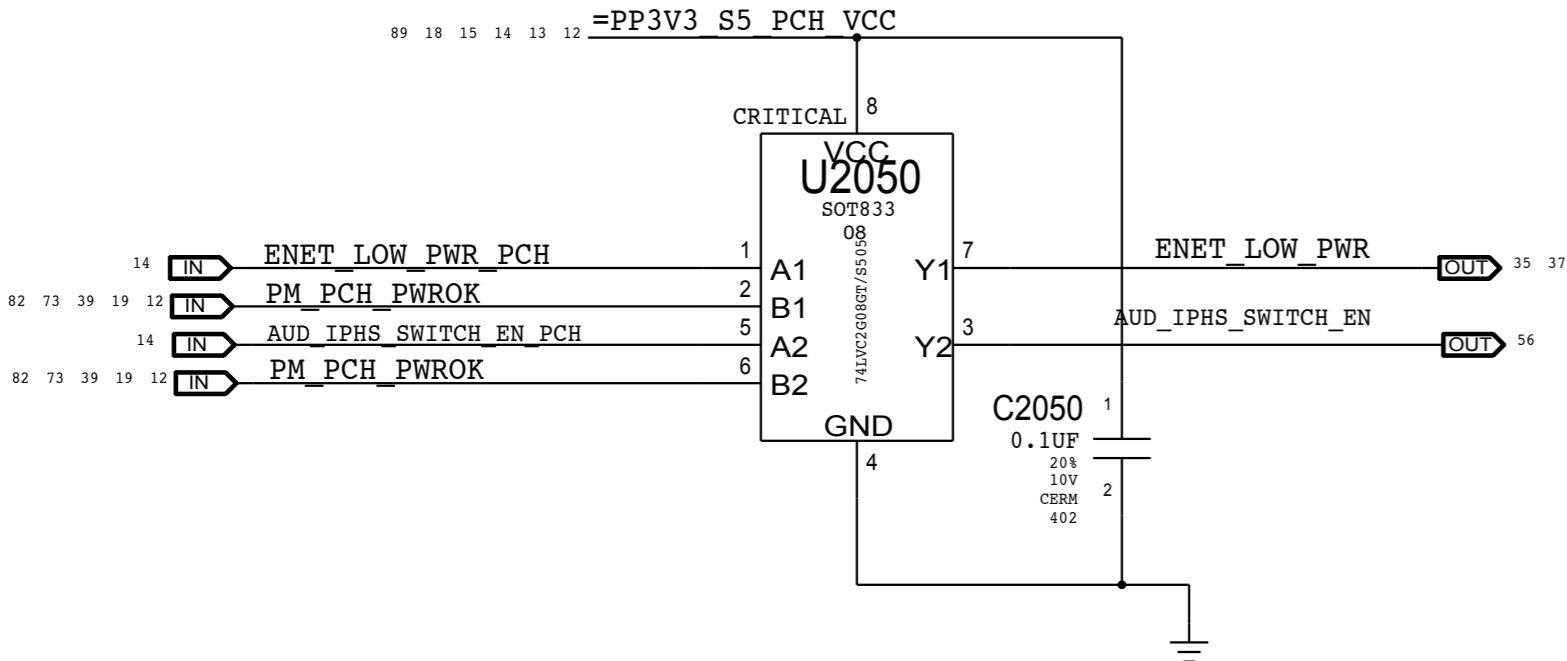
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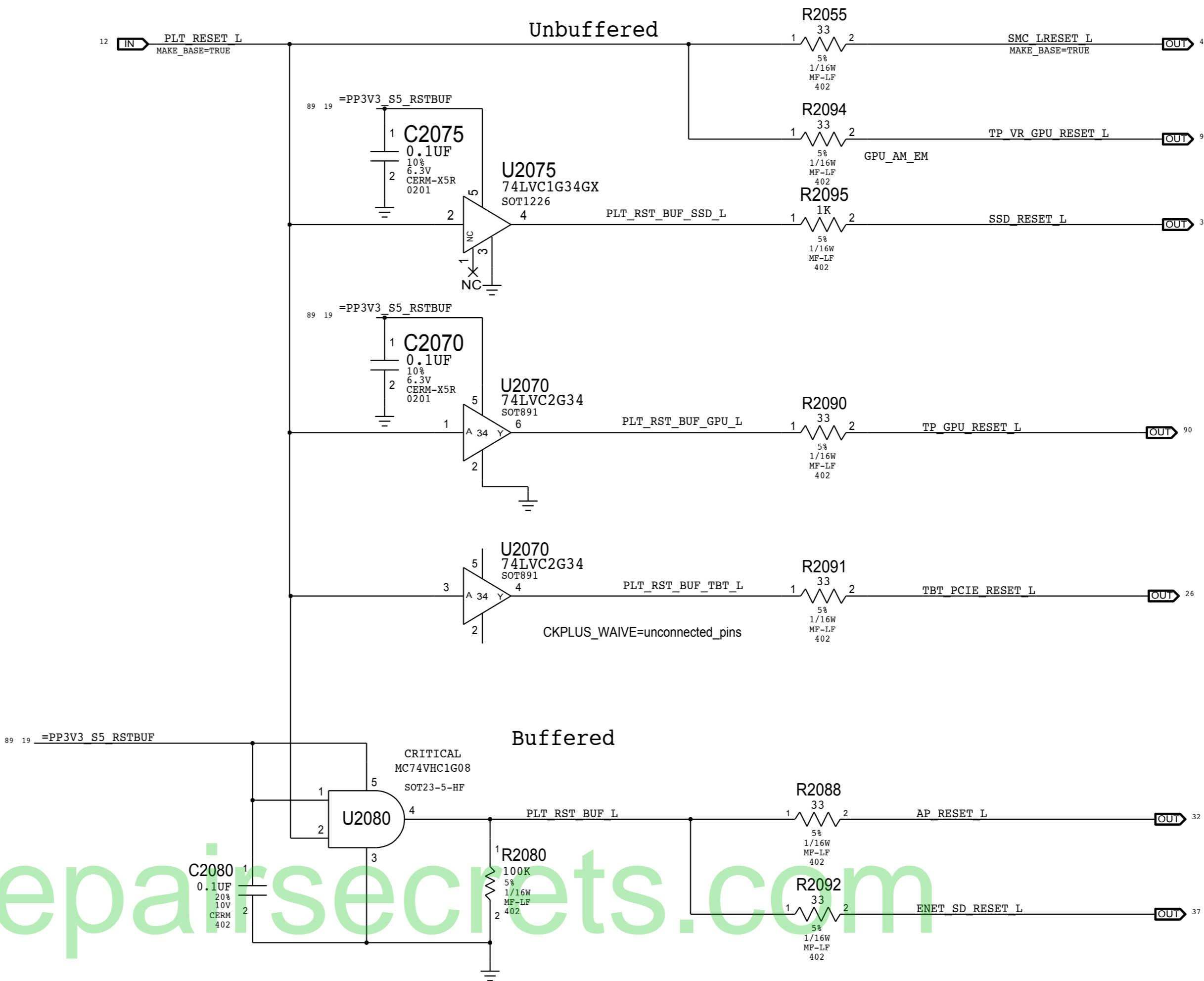
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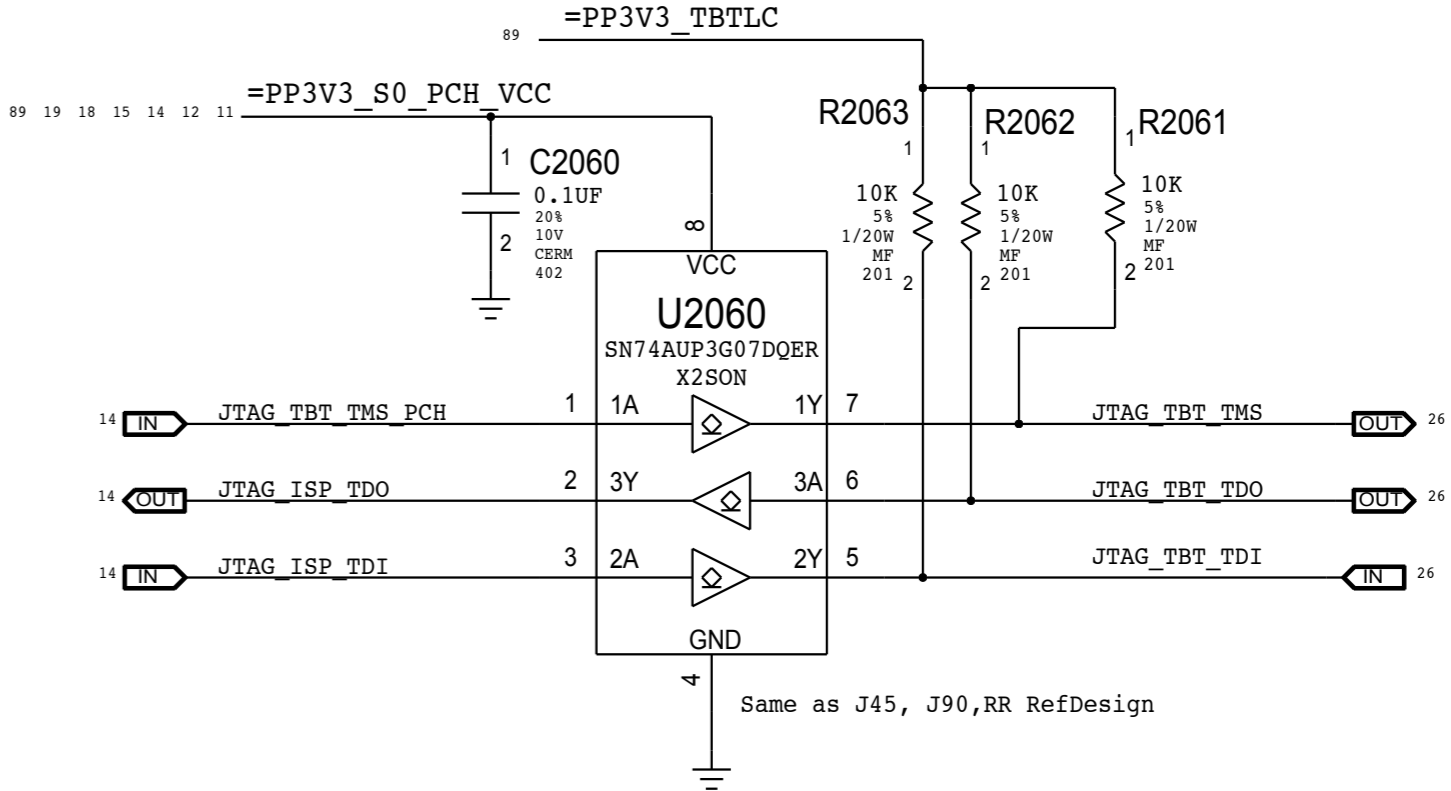
GPIO Glitch Prevention



Platform Reset Connections



TBT_LC can be on when S0 is off and vice-versa.
Isolation ensure no leakage to FR or PCH
U2060 Supports I/Os powered when VCC = 0V




SYNC_MASTER=J16_IG

SYNC_DATE=04/29/2013

PAGE TITLE

CPU & CHIPSET: Project Chipset Support



Apple Inc.

DRAWING NUMBER

051-00673

SIZE

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REVISION

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20 OF 121

SHEET

19 OF 93

D

C

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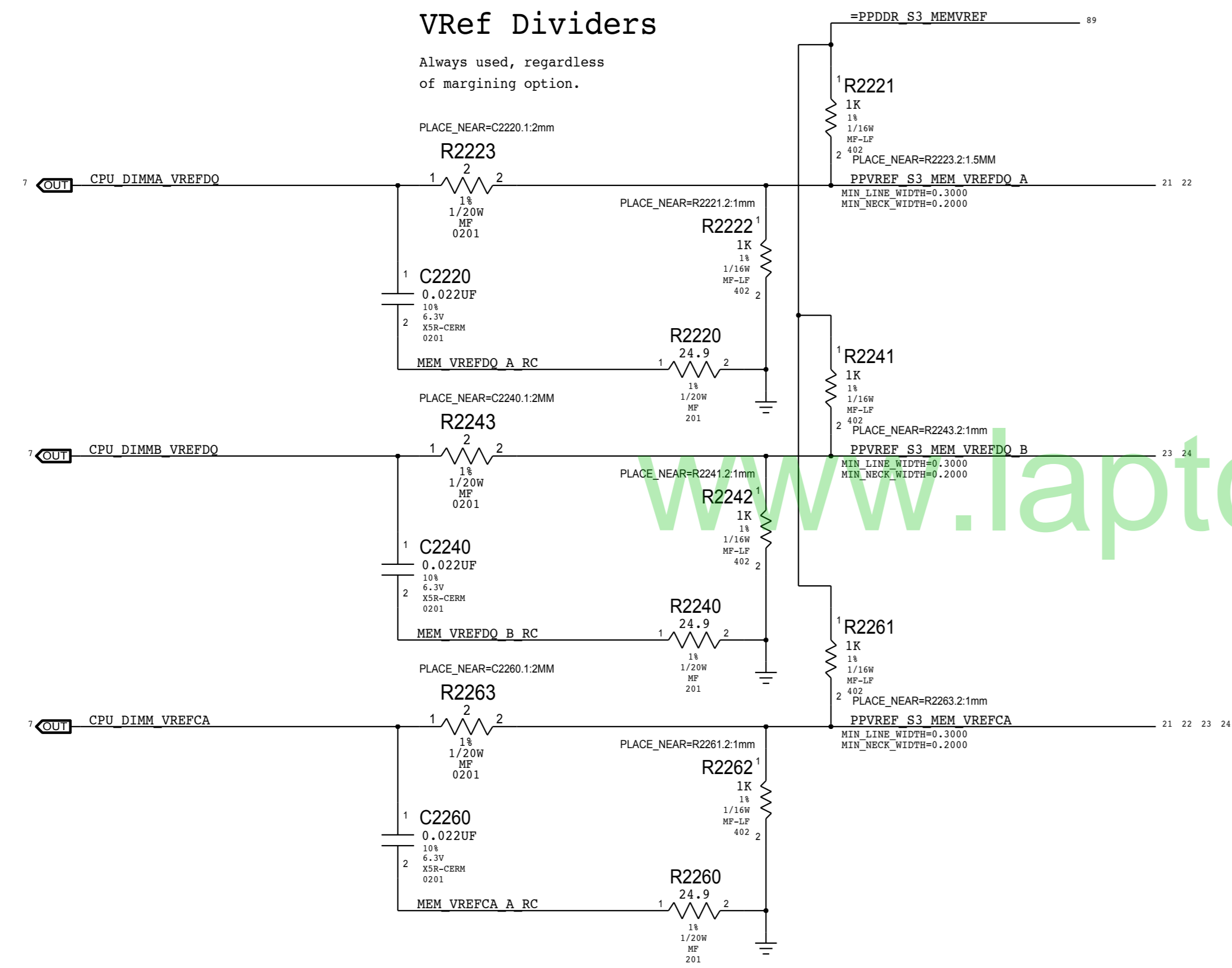
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	0.24.0		
	BRANCH		
	PAGE		
	22 OF 121		
SHEET			
20 OF 93			

Page Notes

Power aliases required by this page:

- *PP1V3_S0_MEM_A

- *PPVDDQ_S3_MEM_A

- *PPDDRVTT_S0_MEM_A

- *PPSPD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:

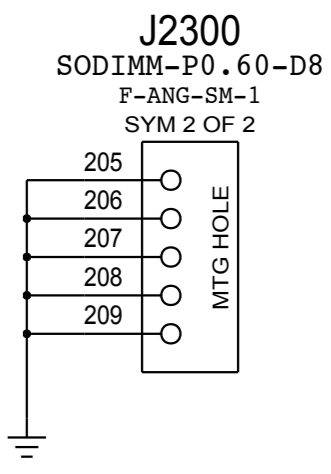
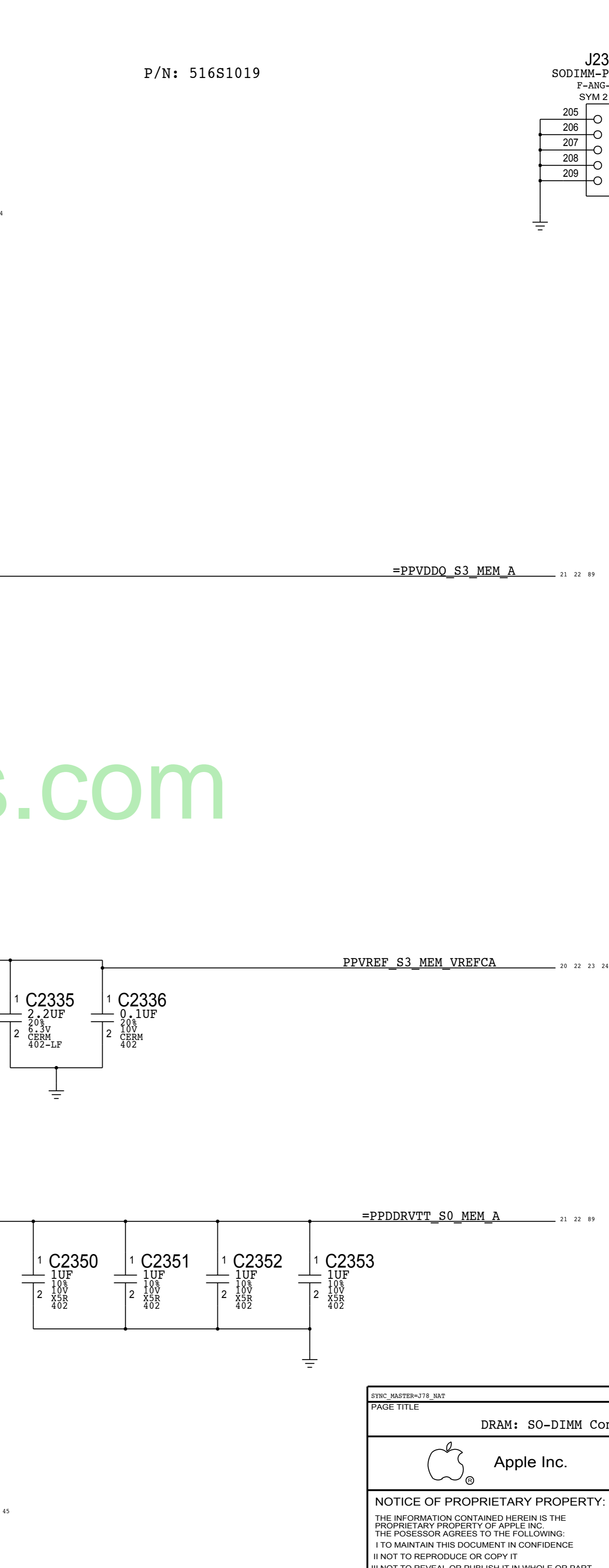
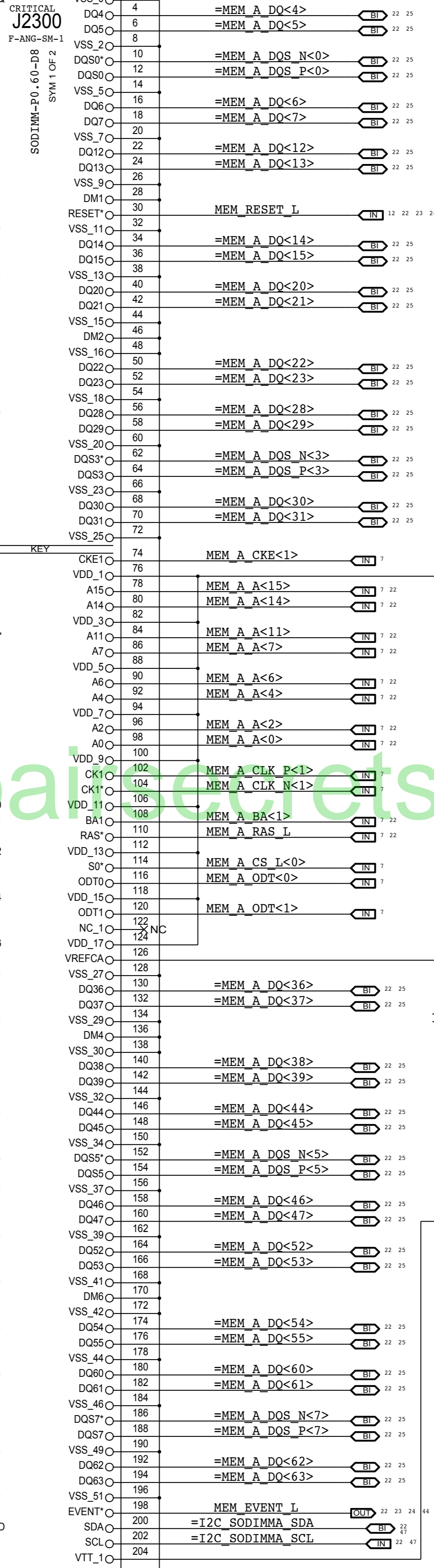
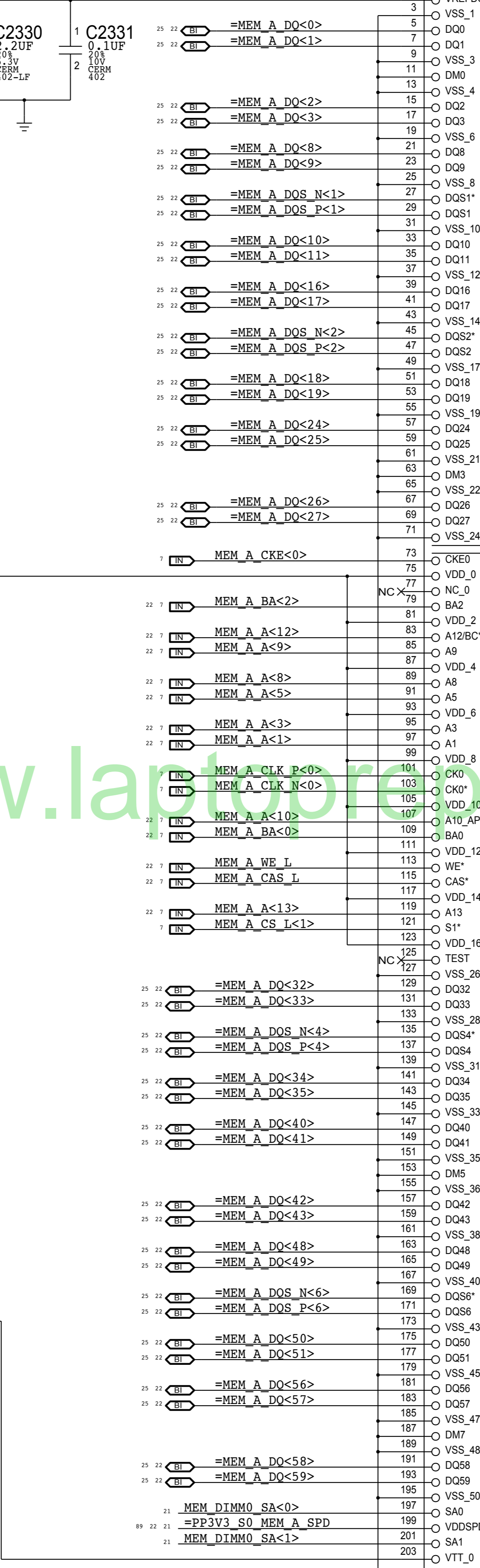
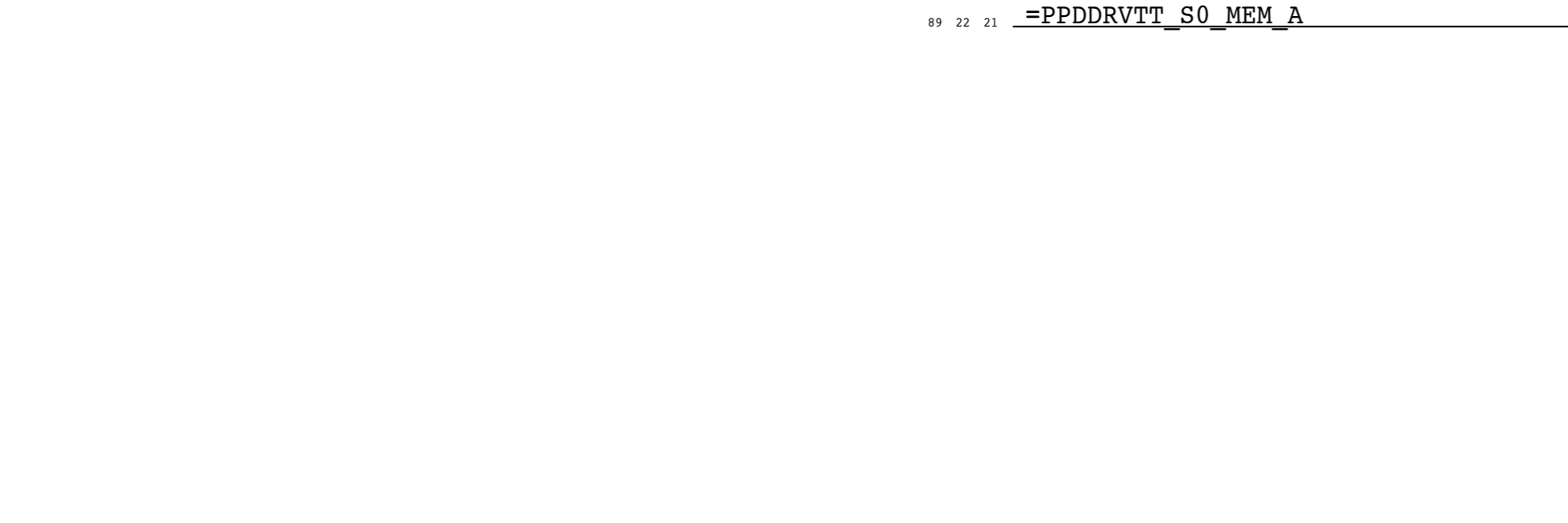
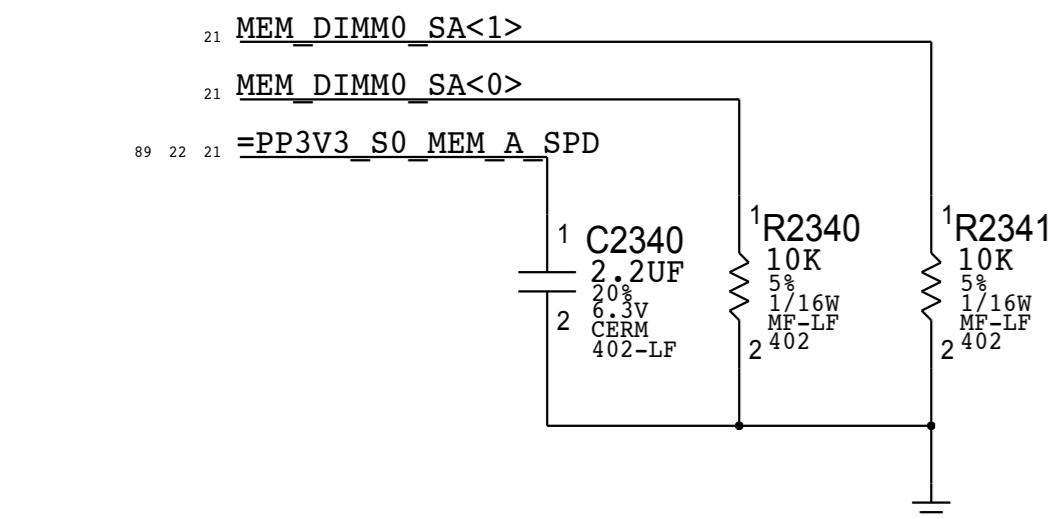
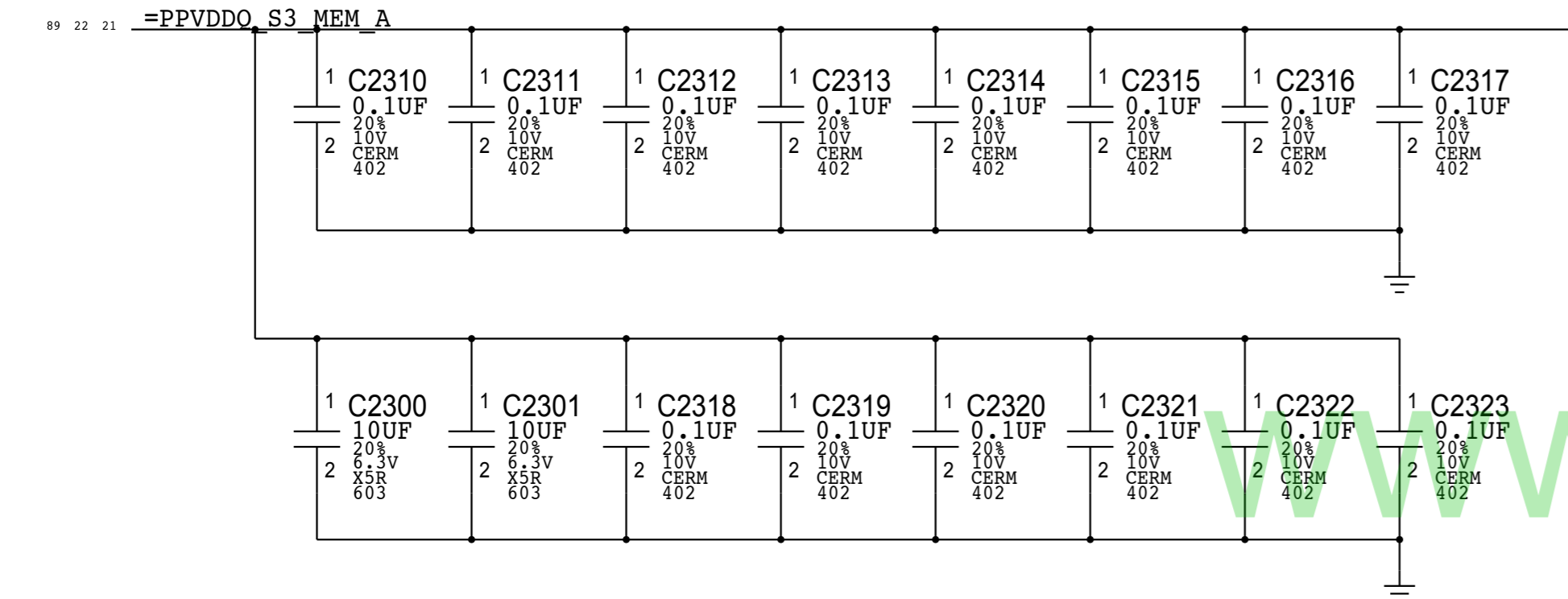
- *I2C_SODIMMA_SCL

- *I2C_SODIMMA_SDA

BOM options provided by this page:

(NONE)

DDR3 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)



SYNC_MASTER=J78_RAT

SYNC_DATE=10/30/2013

DRAM: S0-DIMM Connector A Slot0

Apple Inc.

DRAWING NUMBER051-00673

REVISION0.24.0

BRANCH

PAGE23 OF 121

SHEET21 OF 93

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Page Notes

Power aliases required by this page:

- =PP1V5_S0_MEM_A

- =PPVDDQ_S3_MEM_A

- =PPDDRVTT_S0_MEM_A

- =PPSPD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:

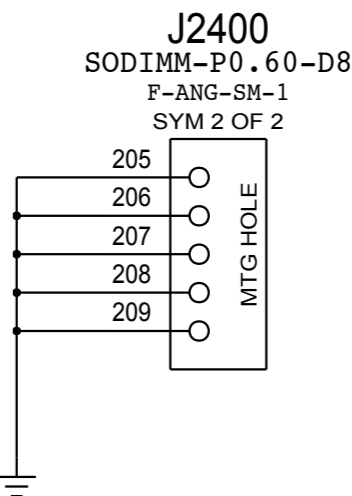
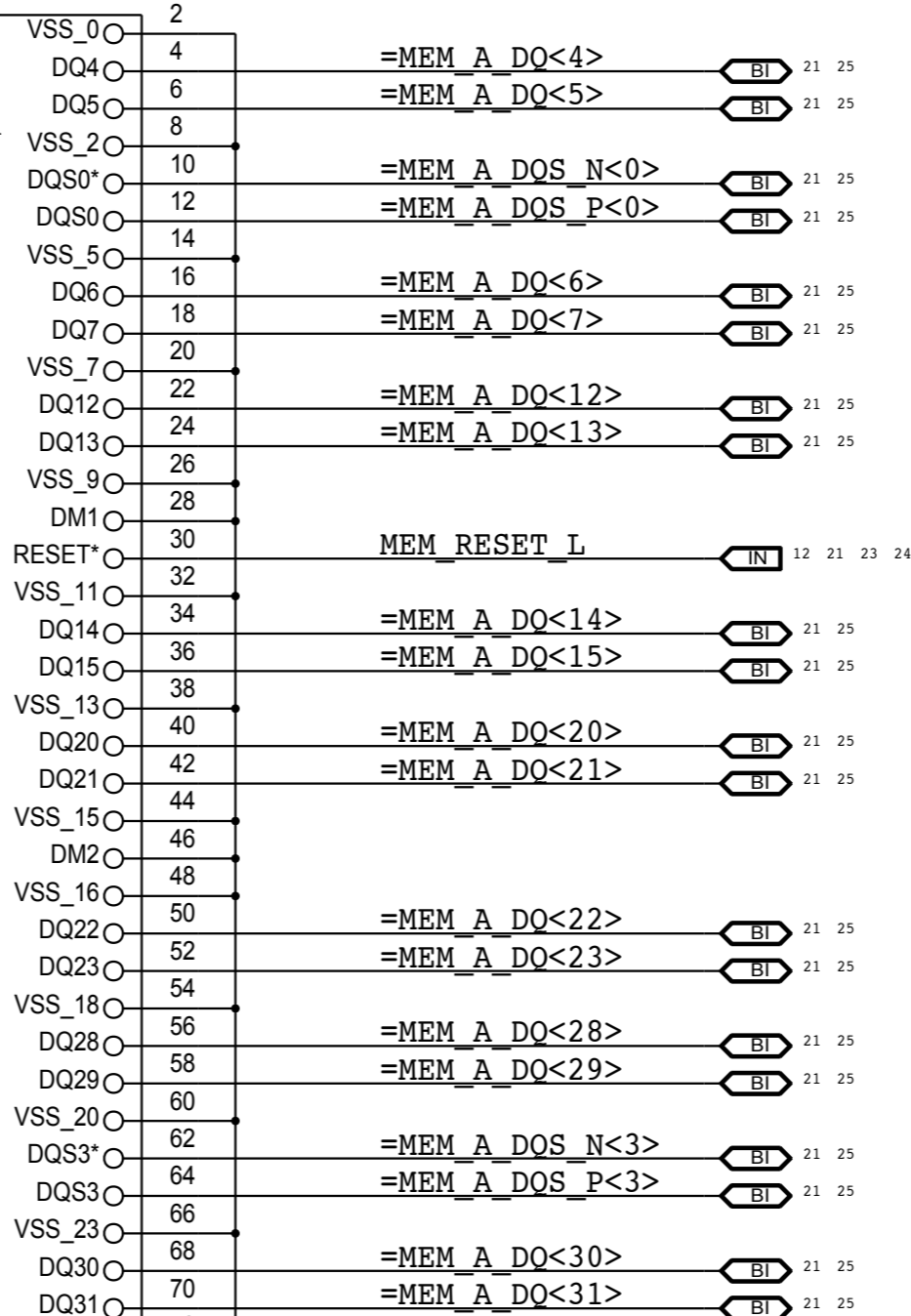
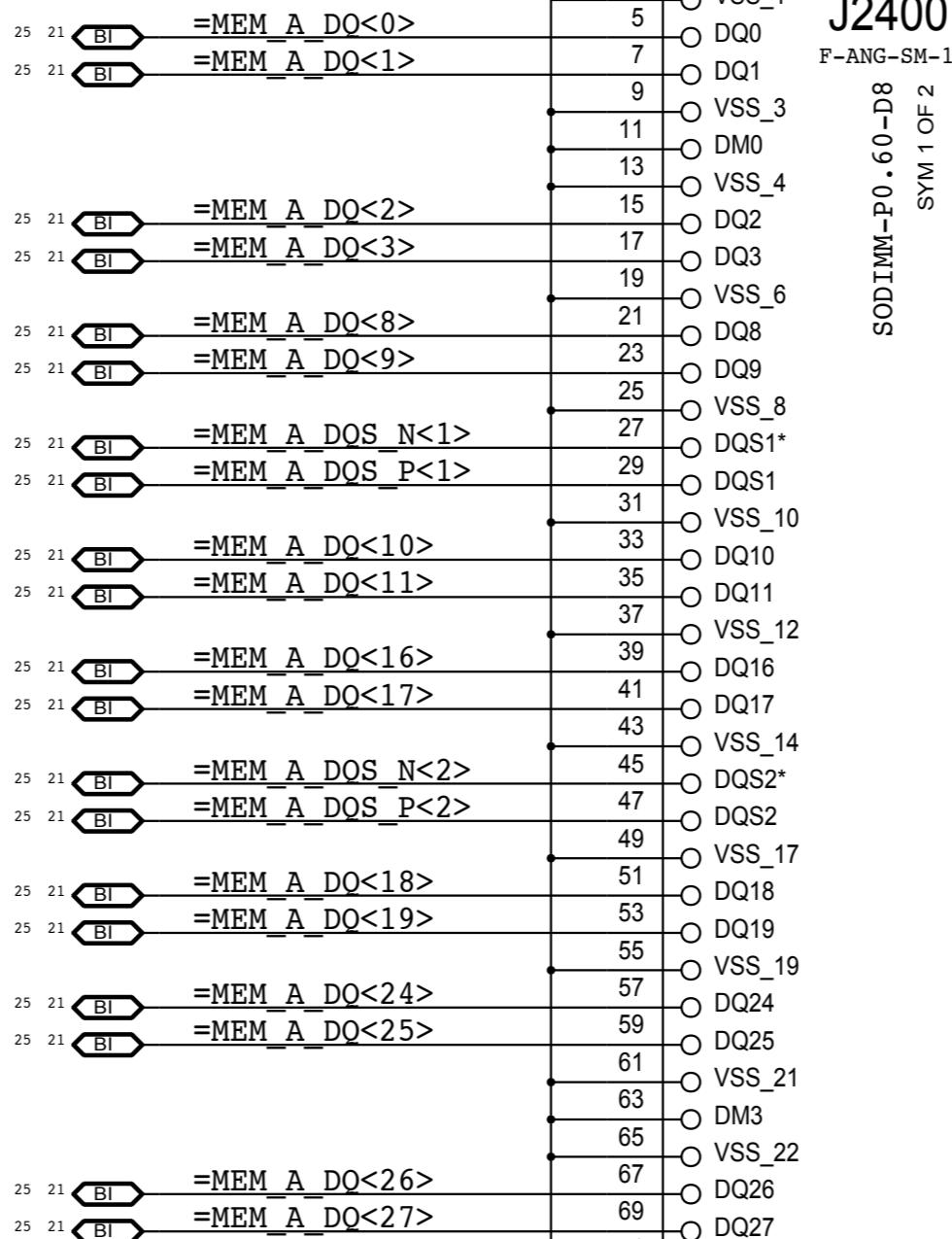
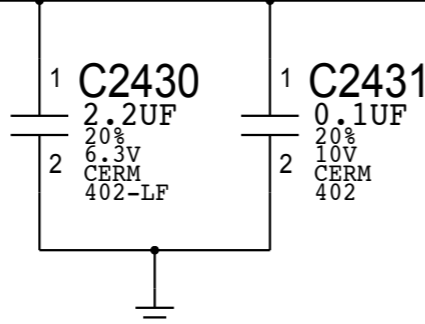
- =I2C_SODIMMA_SCL

- =I2C_SODIMMA_SDA

BOM options provided by this page:

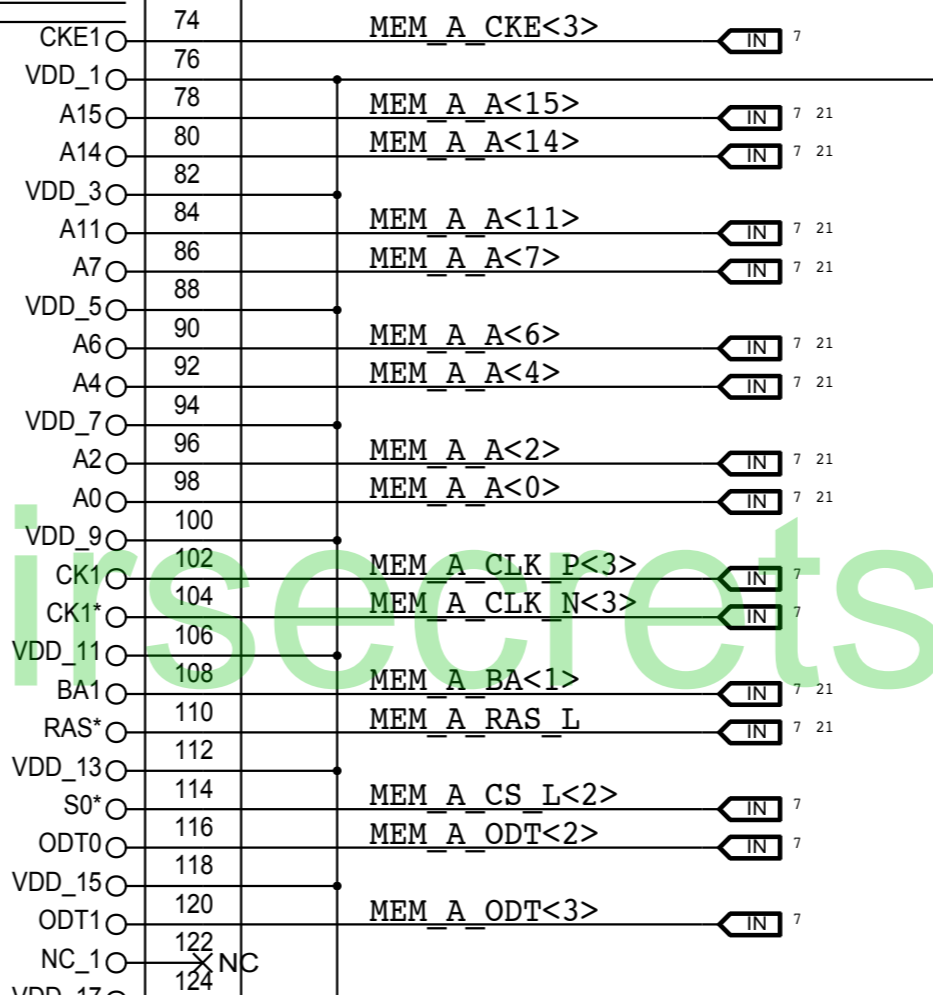
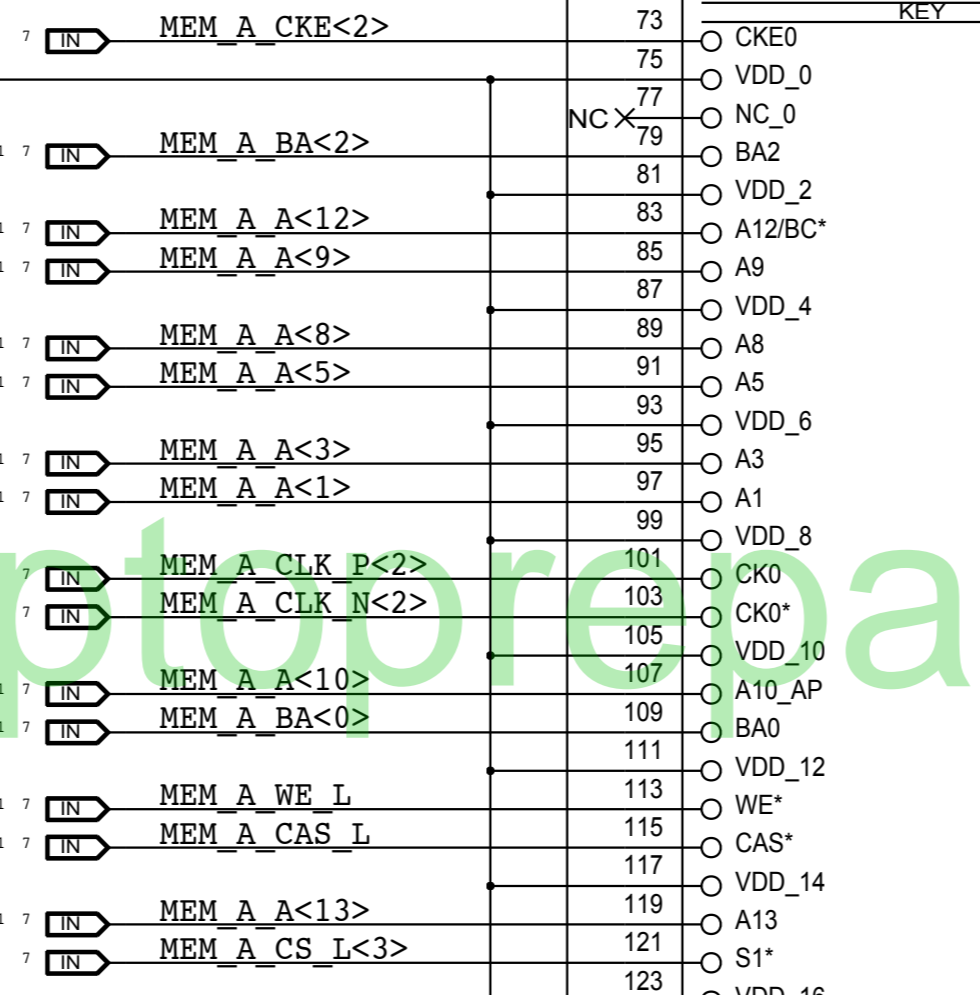
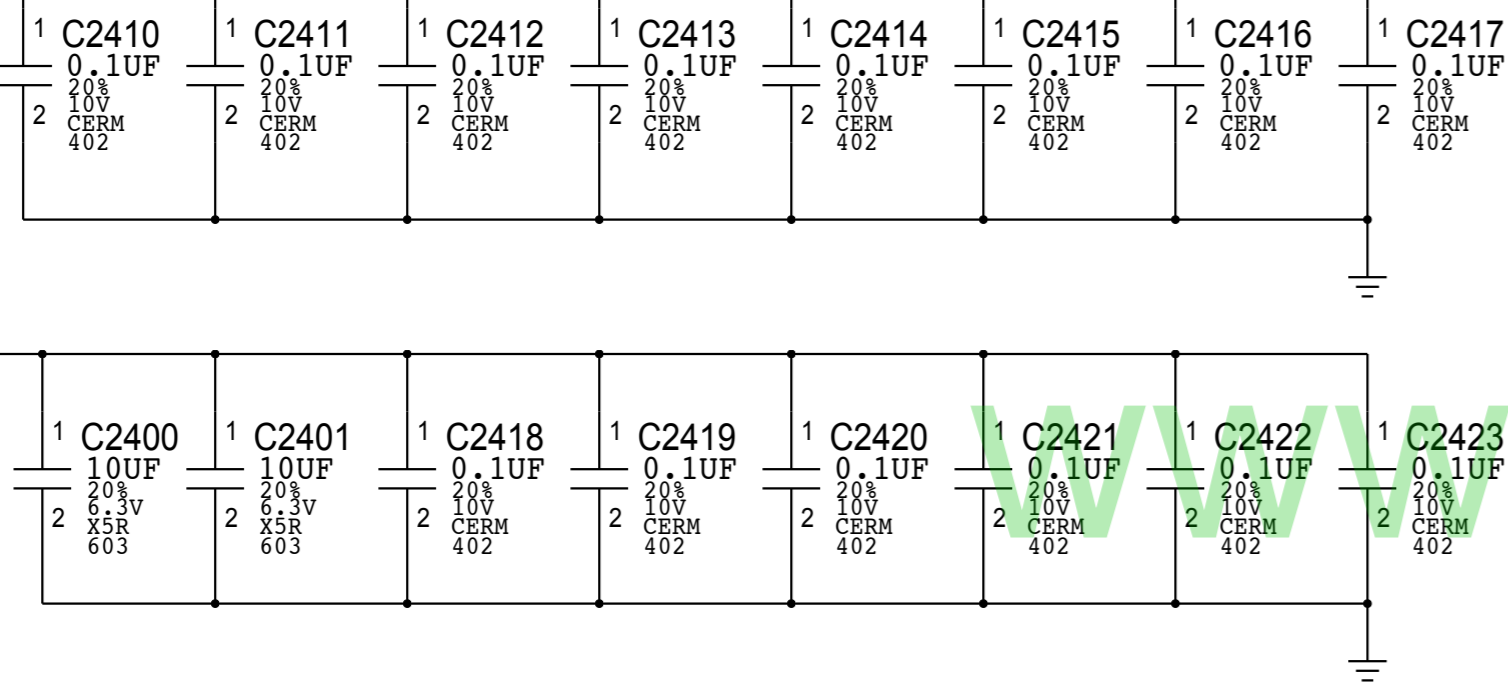
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21 20 PPVREF_S3_MEM_VREFDQ_A



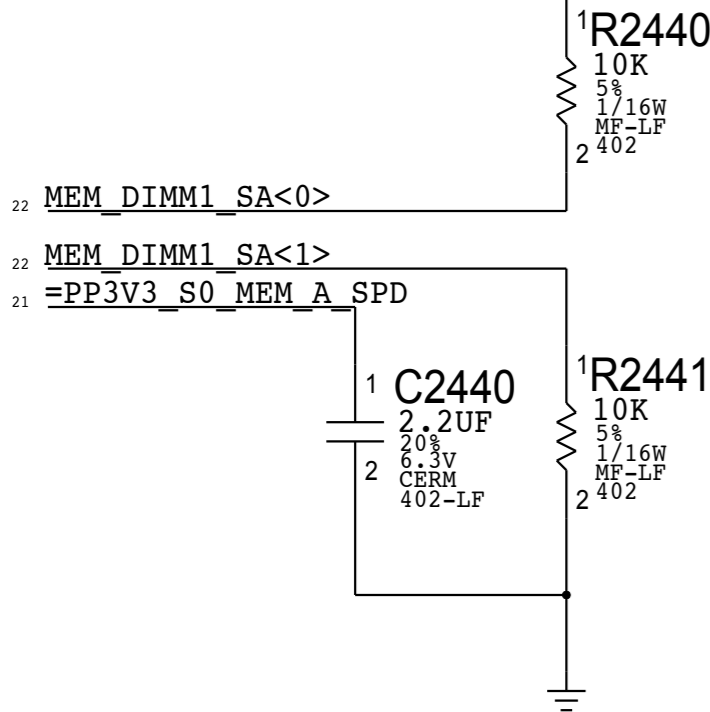
DDR3 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)

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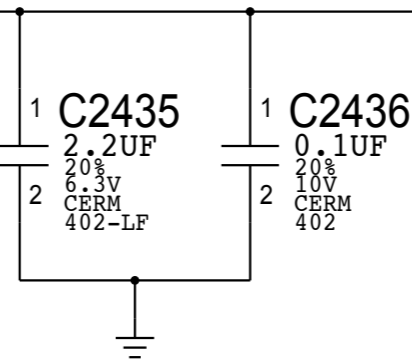


=PPVDDQ_S3_MEM_A

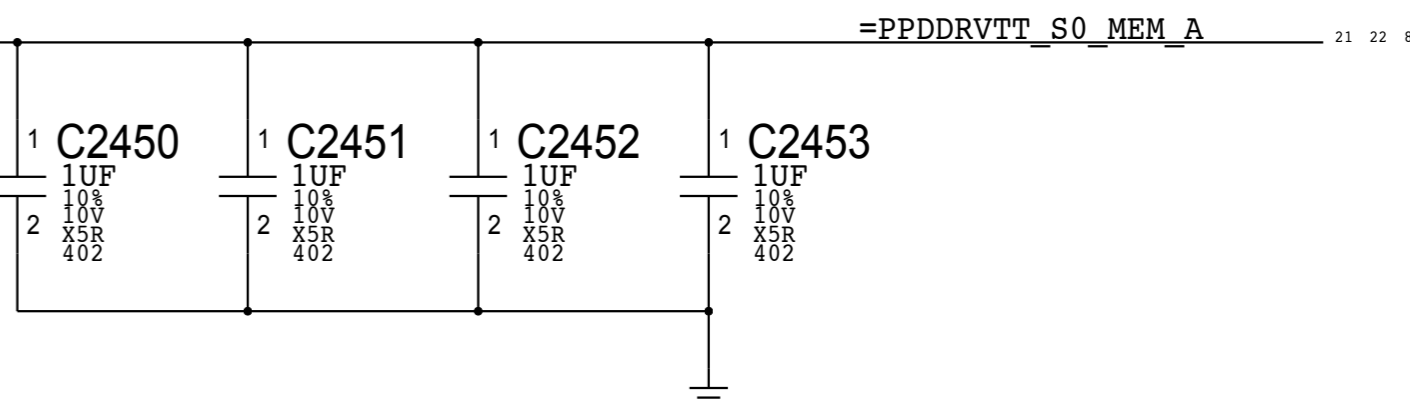
89 22 21 =PP3V3_S0_MEM_A_SPD



89 22 21 =PPDDRVTT_S0_MEM_A



PPVREF_S3_MEM_VREFCA



SYNC_MASTER=J78_RAT

SYNC_DATE=10/30/2013

DRAM: SO-DIMM Connector A Slot1

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DRAWING NUMBER

051-00673

REVISION

0.24.0

BRANCH

PAGE

24 OF 121

SHEET

22 OF 93

SIZE

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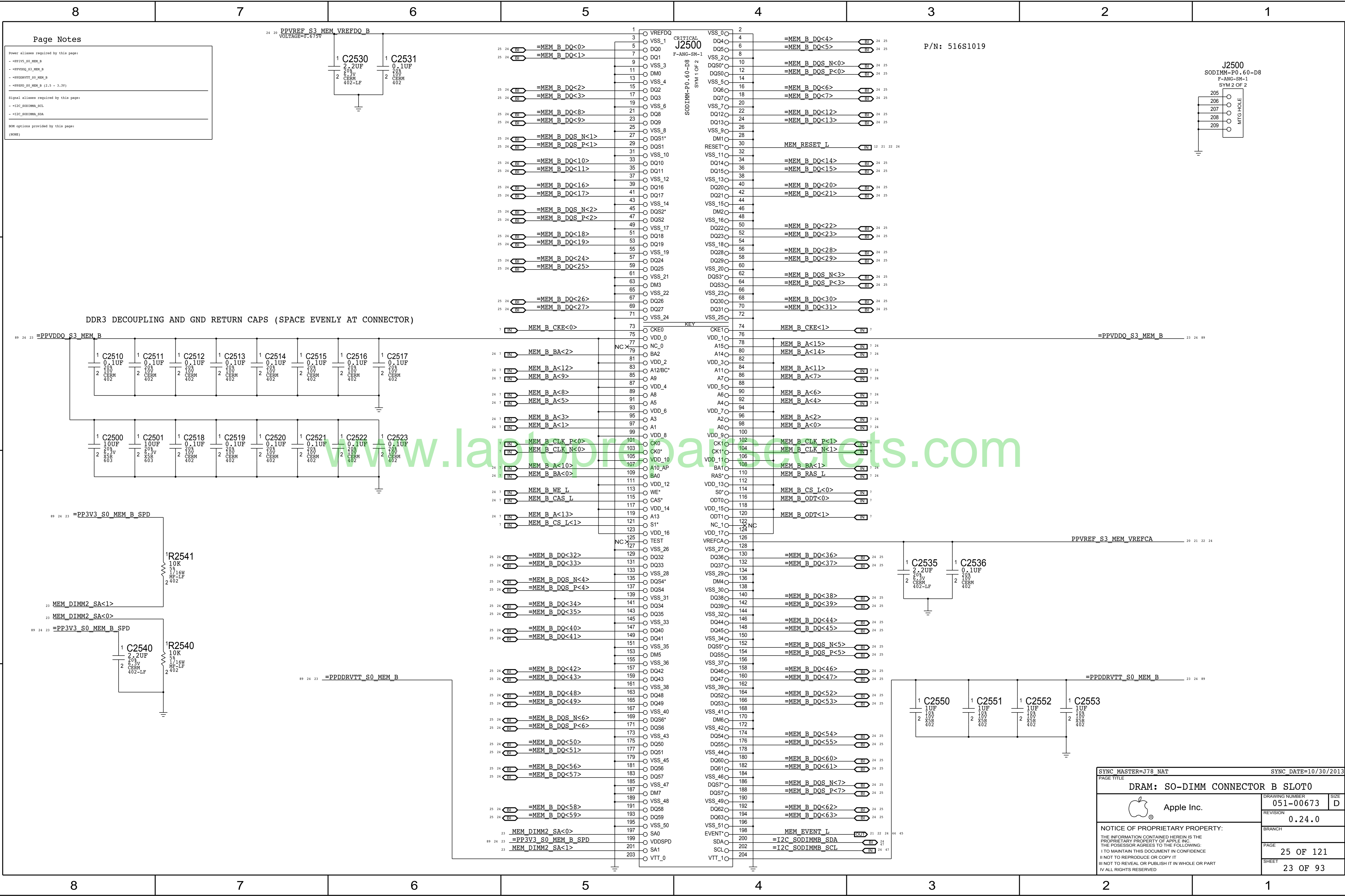
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Page Notes

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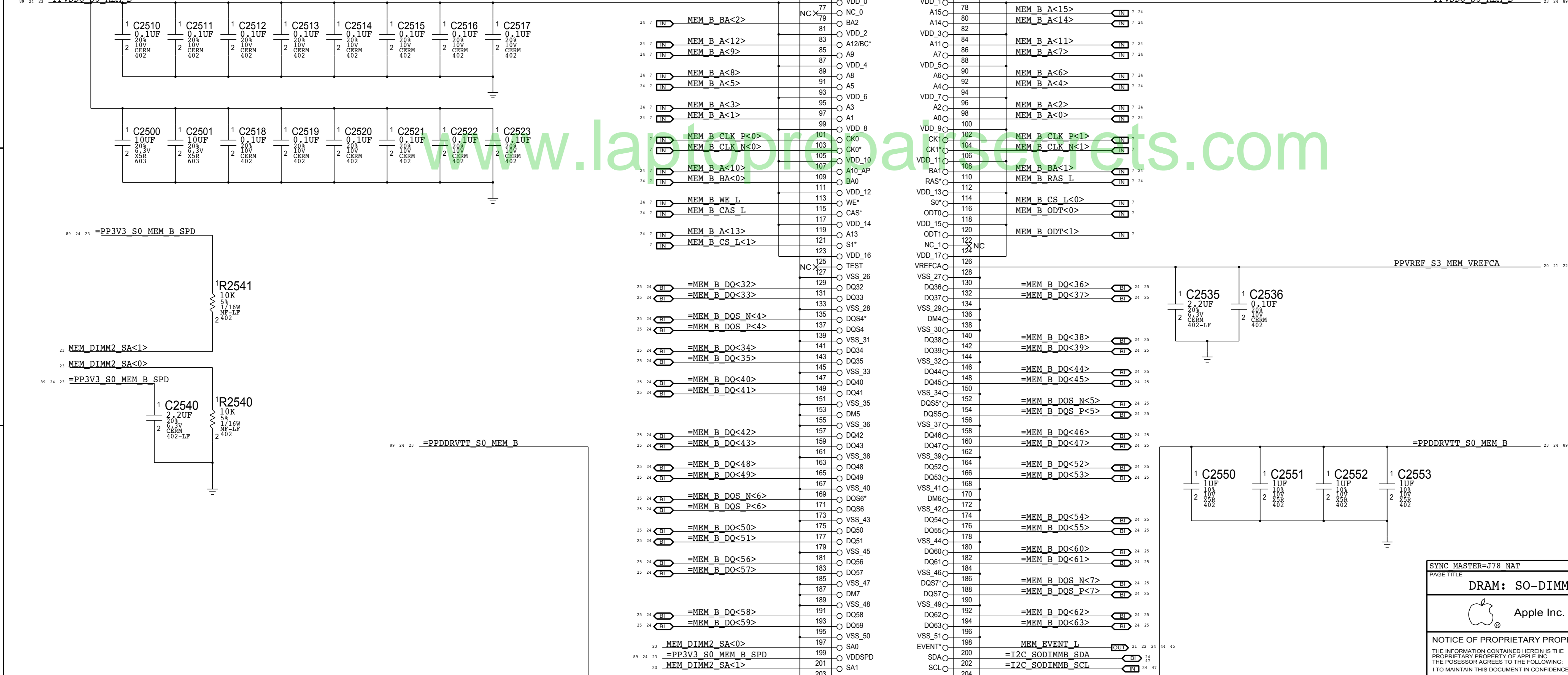
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- *PPVDDQ_S3_MEM_B
- *PPDDRVTT_S0_MEM_B
- *PPREF_S0_MEM_B (2.5 - 3.3V)

Signal aliases required by this page:

- *I2C_S0DIMM_SCL
- *I2C_S0DIMM_SDA

BOM options provided by this page:

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Page Notes

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Power aliases required by this page:

- PP1V1_S0_MEM_B
- PP1V0Q_Q3_MEM_B
- PPFCORQTT_S0_MEM_B
- PPSFQ_Q0_MEM_B (2.5 - 3.3V)
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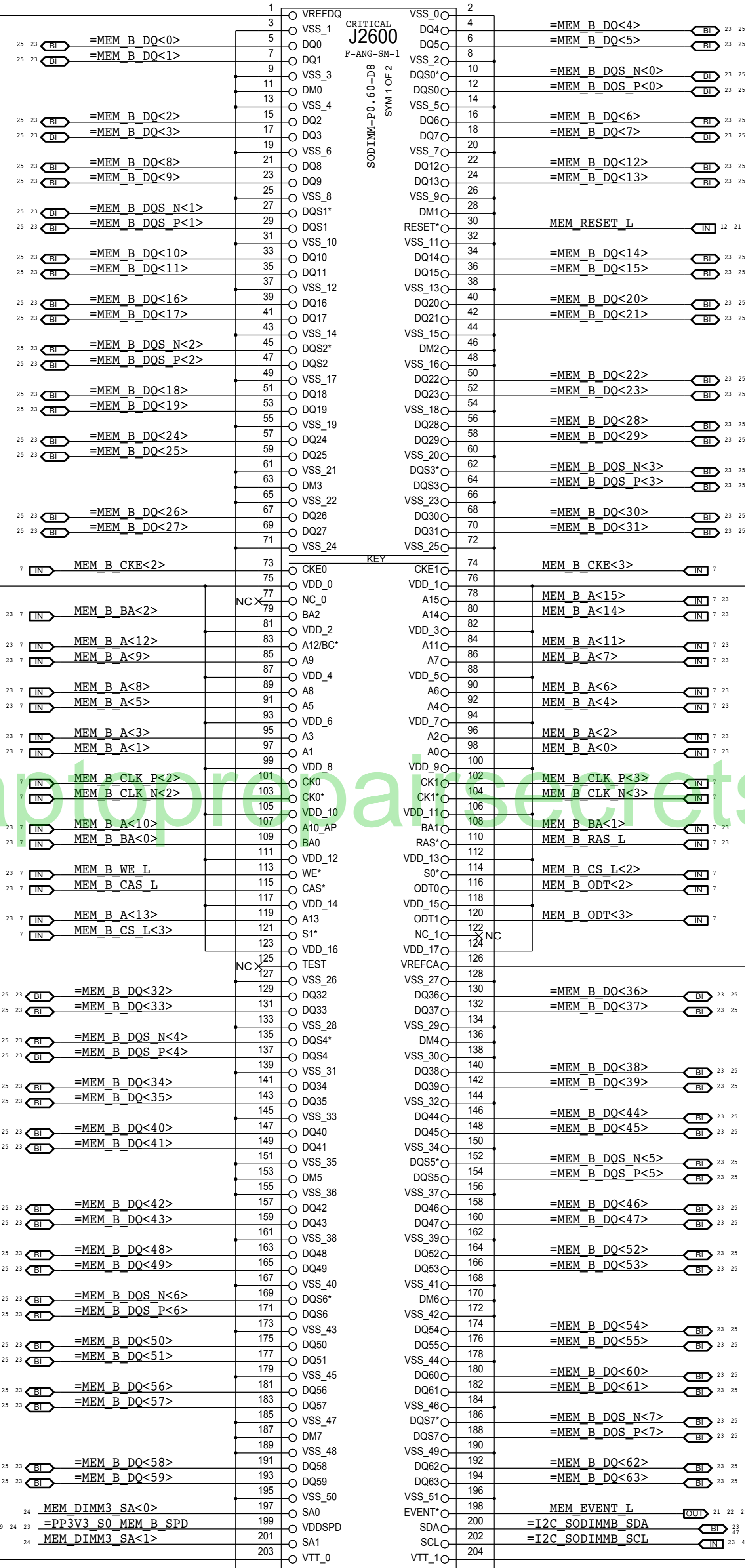
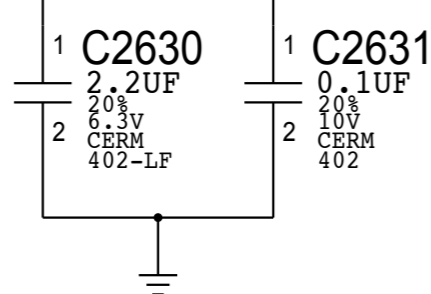
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Signal aliases required by this page:

- I2C_S0DINMA_SCL
- I2C_S0DINMA_SDA
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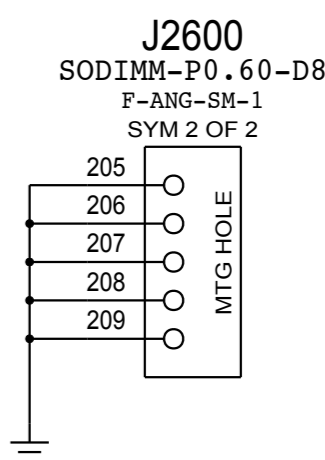
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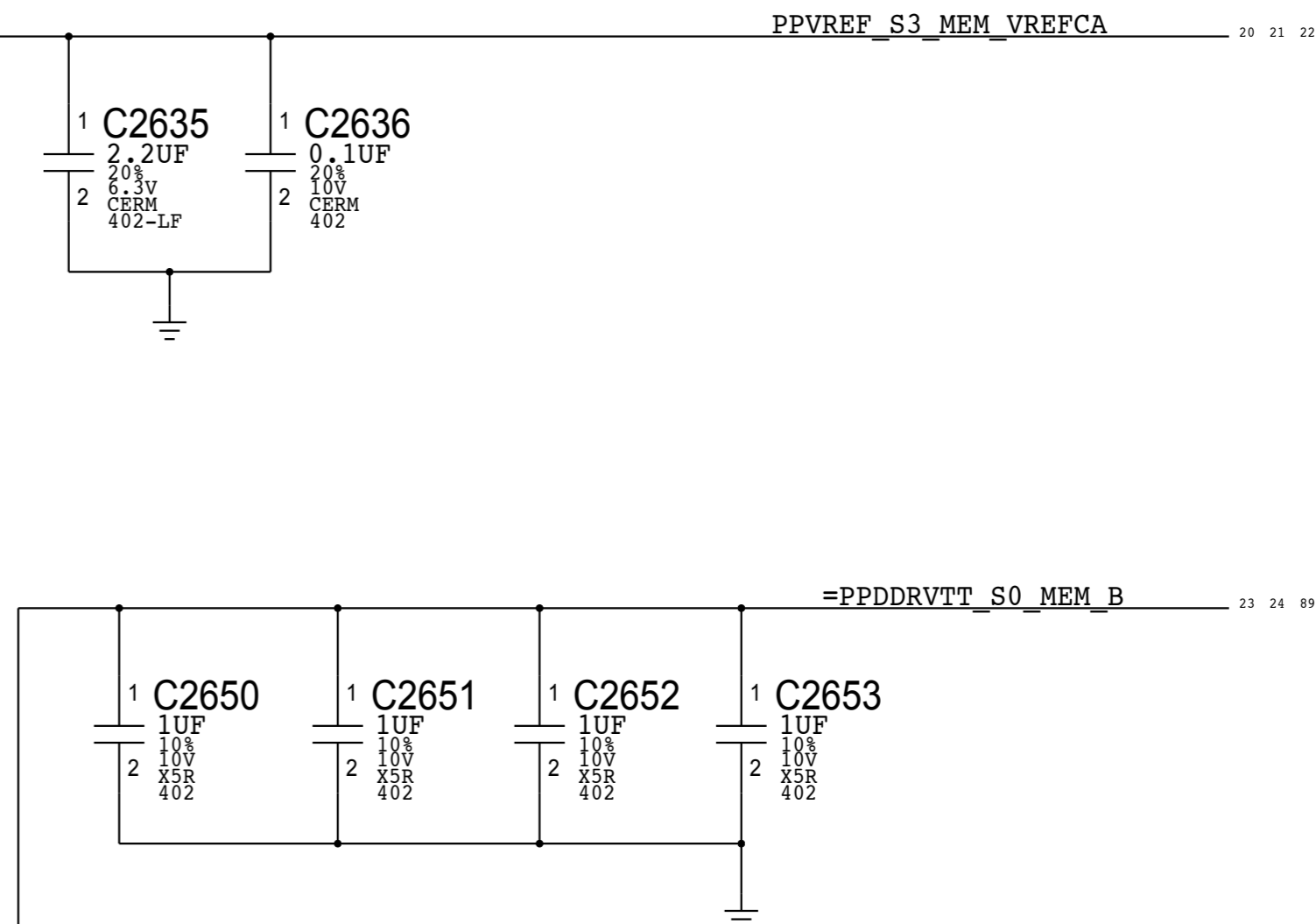
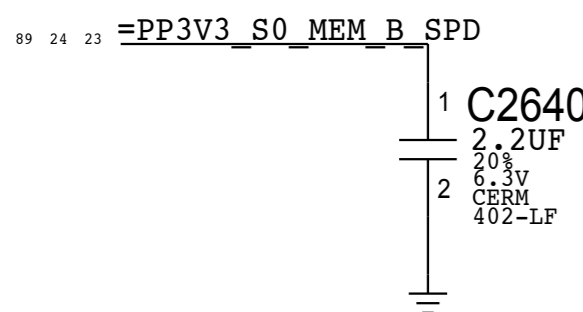
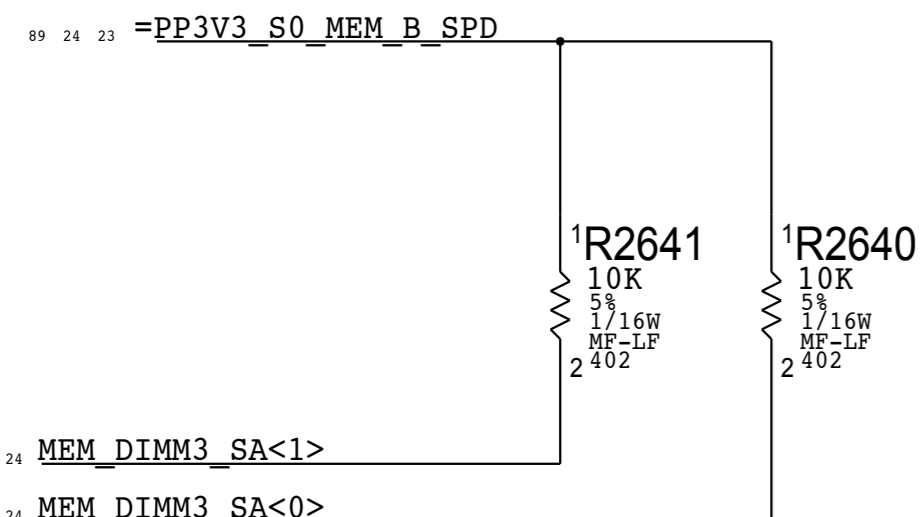
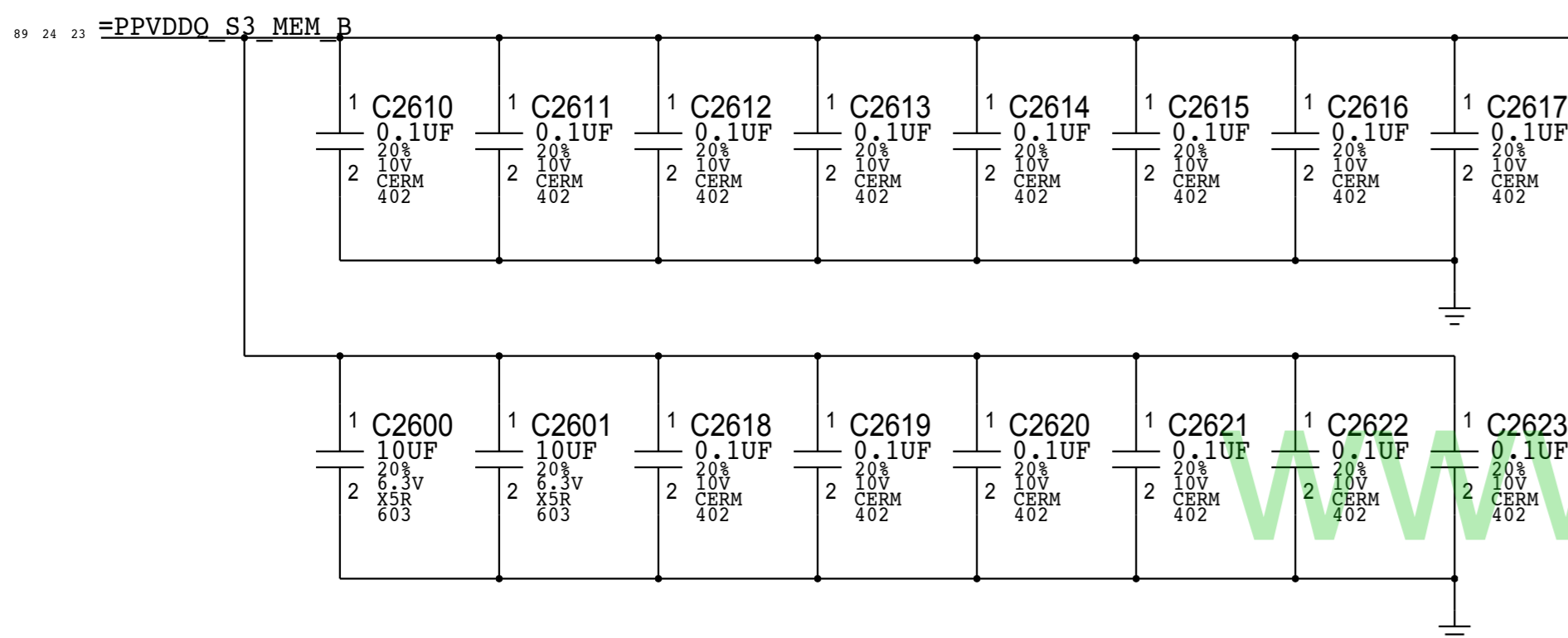
23 20 PPVREF S3 MEM VREFDQ B
VOLTAGE=0.675V




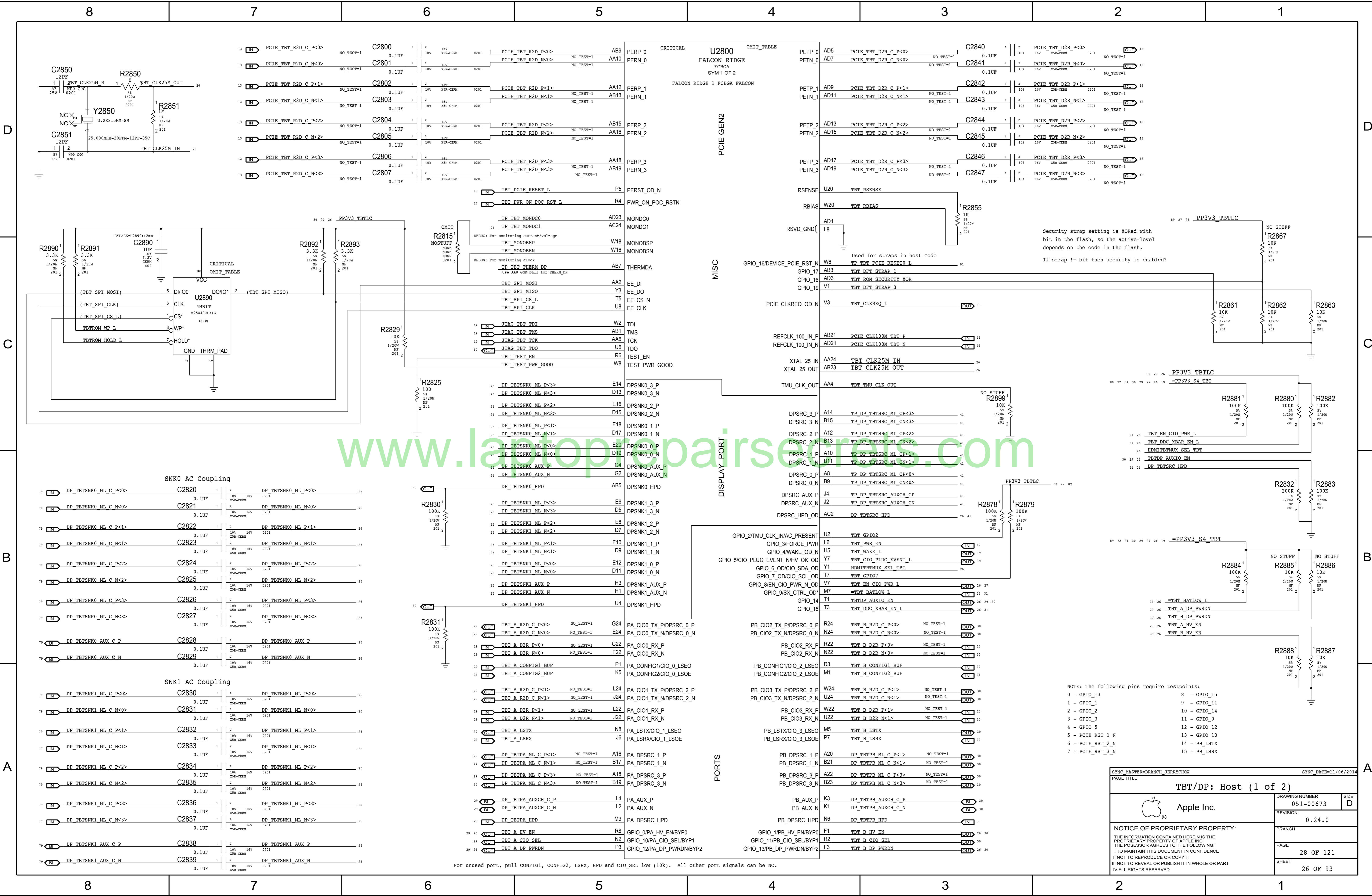
P/N: 516S1019



DDR3 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)

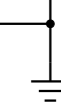



SYNC MASTER=J78 NAT PAGE TITLE		SYNC DATE=10/30/2013	
DRAM: SO-DIMM CONNECTOR B SLOT1			
 Apple Inc.		DRAWING NUMBER 051-00673	SIZE D
		REVISION 0.24.0	
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NOTE: The following pins require testpoints:

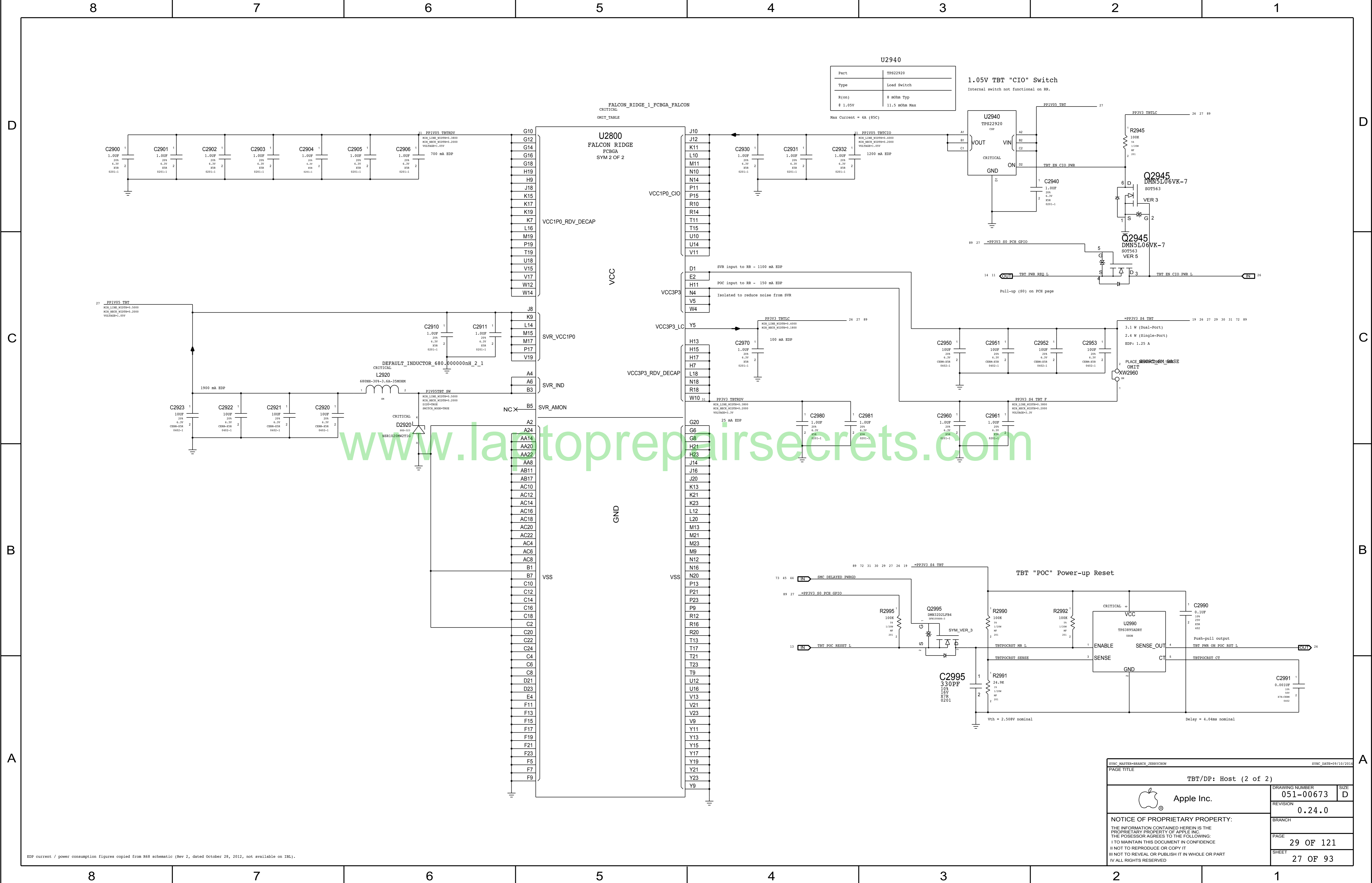
0 - GPIO_13	8 - GPIO_15
1 - GPIO_1	9 - GPIO_11
2 - GPIO_2	10 - GPIO_14
3 - GPIO_3	11 - GPIO_0
4 - GPIO_5	12 - GPIO_12
5 - PCIE_RST_1_N	13 - GPIO_10
6 - PCIE_RST_2_N	14 - PB_L5TX
7 - PCIE_RST_3_N	15 - PB_L5RX



SYNC_MASTER=BRANCH_JERRYCHOW		SYNC_DATE=11/06/2014	
PAGE TITLE			
TBT/DP: Host (1 of 2)			
 Apple Inc.	DRAWING NUMBER		SIZE
	051-00673		D
	REVISION		
	0.24.0		
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		28 OF 121	
		SHEET	
		26 OF 93	

NOTE: The following pins require testpoints:
0 - GPIO_13
1 - GPIO_1
2 - GPIO_2
3 - GPIO_3
4 - GPIO_5
5 - PCIE_RST_1_N
6 - PCIE_RST_2_N
7 - PCIE_RST_3_N
8 - GPIO_15
9 - GPIO_11
10 - GPIO_14
11 - GPIO_0
12 - GPIO_12
13 - GPIO_10
14 - PB_LSTX
15 - PB_LSRX

For unused port, pull CONFIG1, CONFIG2, LSRX, HPD and CIO_SEL low (10k). All other port signals can be NC.



EDP current / power consumption figures copied from R60 schematic (Rev 2, dated October 28, 2012, not available on IBU).

8		7		6		5		4		3		2		1		
D	<div>Page Notes</div> <div><div>Power aliases required by this page:<ul style="list-style-type: none">=PPVIN_SW_TBTBST (8-13V Boost Input)=PP15V_TBT_REG (15V Boost Output)=PP3V3_TBT_P3V3TBTFFET (3.3V FET Input)=PP3V3_TBT_FET (3.3V FET Output)=PP3V3_S0_TBTPOWERCTL=PP1V05_TBT_P1V05TBTFFET (1.05V FET Input)=PP1V05_TBT_FET (1.05V FET Output)</div><div>Signal aliases required by this page:<ul style="list-style-type: none">=TBT_CLKREQ_L=TBT_RESET_L</div><div>BOM options provided by this page: TBTBST:Y - Stuffs 15V boost circuitry.</div></div>															D
C														C		
B														B		
A														A		
8		7		6		5		4		3		2		1		

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Thunderbolt: Power Support

DRAWING NUMBER

051-00673

REVISION

0.24.0

PAGE

30 OF 121


SHEET

28 OF 93

SYNC MASTER=J78 JERRY

SYNC DATE=10/09/2013

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SYNC_MASTER=J78 JERRY		SYNC_DATE=10/09/2013	
PAGE TITLE			
Thunderbolt: Power Support			
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		SIZE D	
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		BRANCH	
		PAGE	30 OF 121
		SHEET	28 OF 93

D

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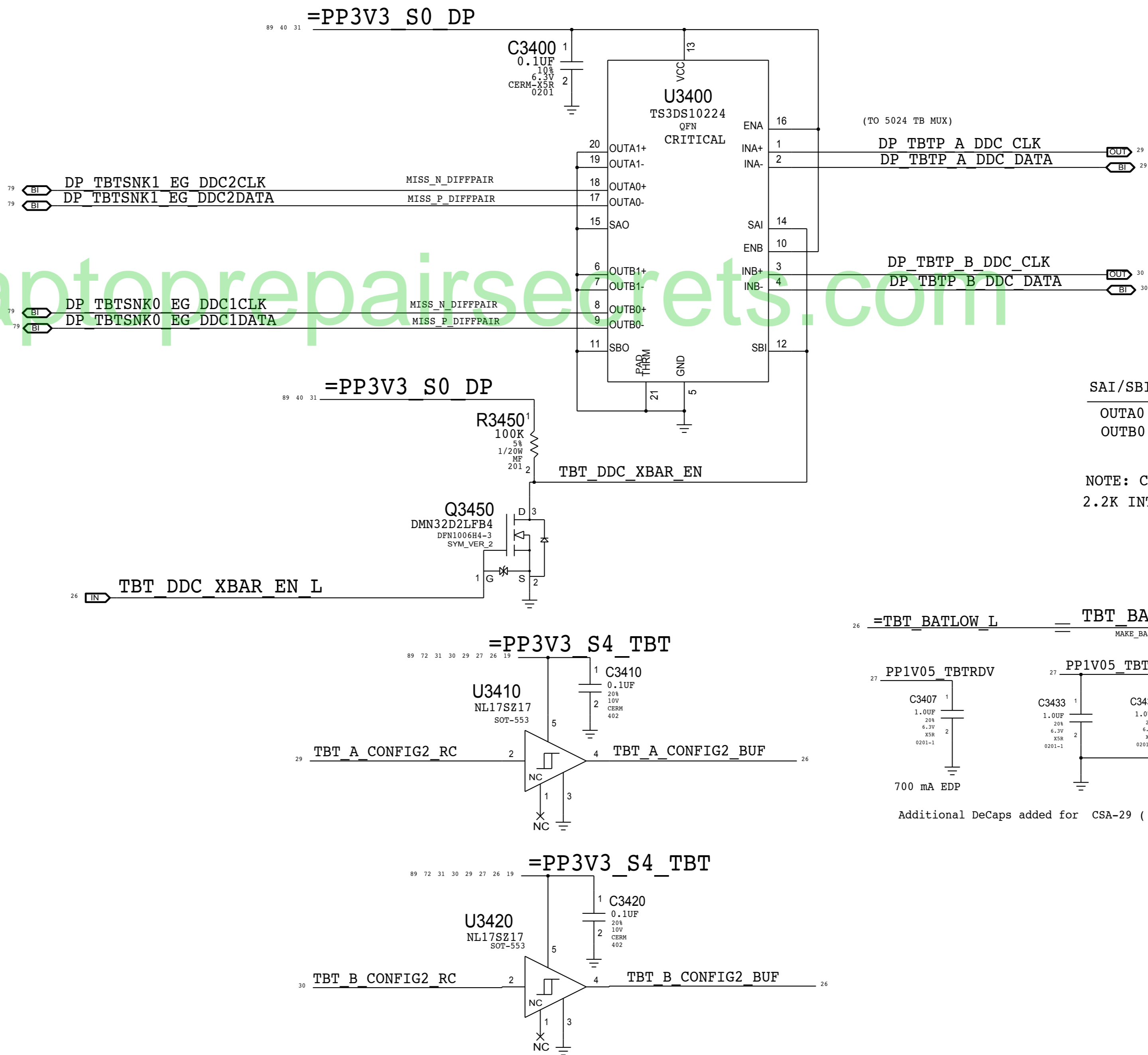
D

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Dual-Port Host DDC Crossbar



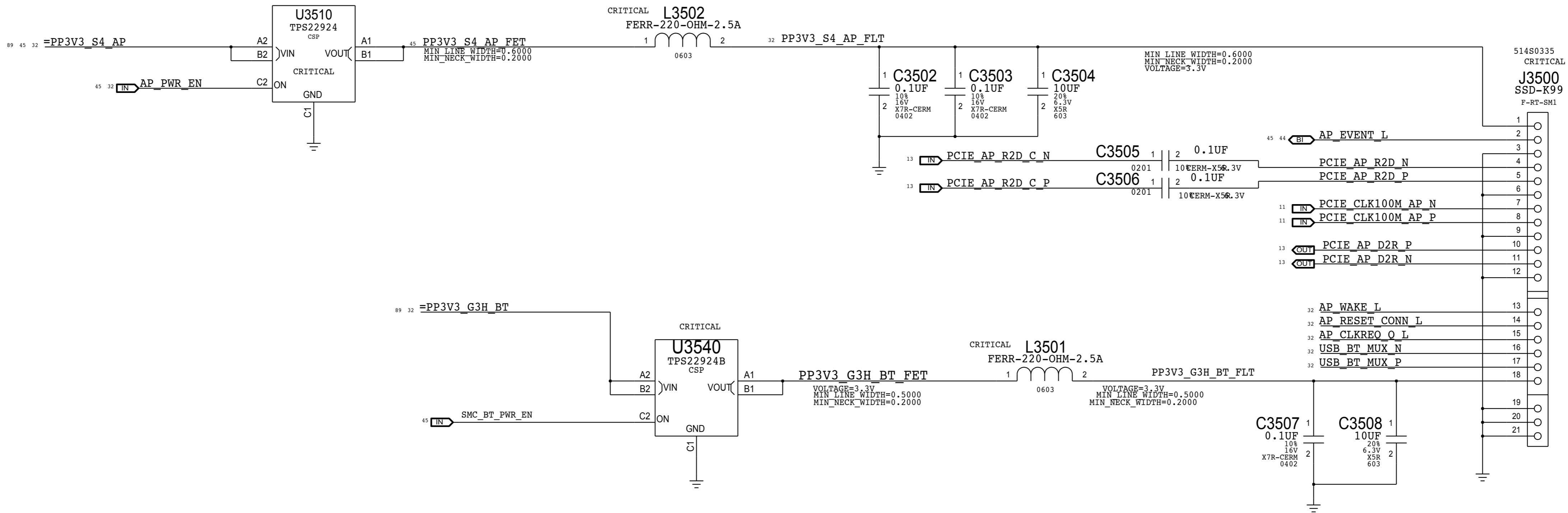
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OUTA0 =	INB	INA
OUTB0 =	INA	INB

NOTE: CABLE ADAPTERS ARE REQUIRED TO HAVE 2.2K INTERNAL PULL-UPS.

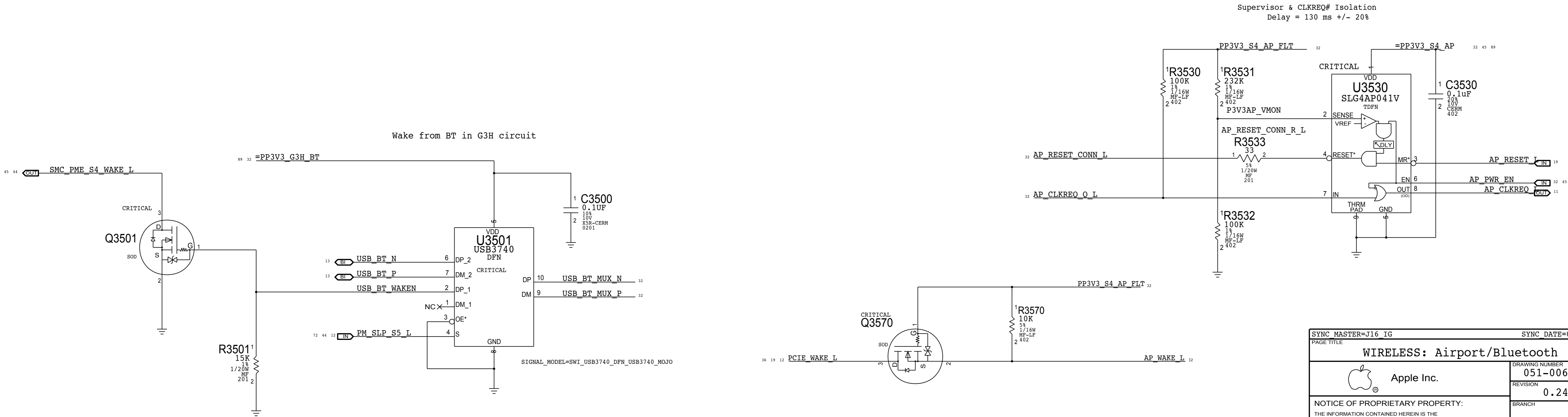
SYNC_MASTER=BRANCH JERRYCHOW		SYNC_DATE=11/05/2014	
PAGE TITLE			
TBT/DP: DDC Crossbar			
 Apple Inc.	DRAWING NUMBER	051-00673	SIZE D
	REVISION	0.24.0	
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		SHEET 31 OF 93	

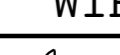
AP & BT Load Switch	
SWITCH	TPS22924B
CHANNEL	N-TYPE
RDS(ON)	18.4 MOHM @3.3V
LOADING	2 A (SDP)

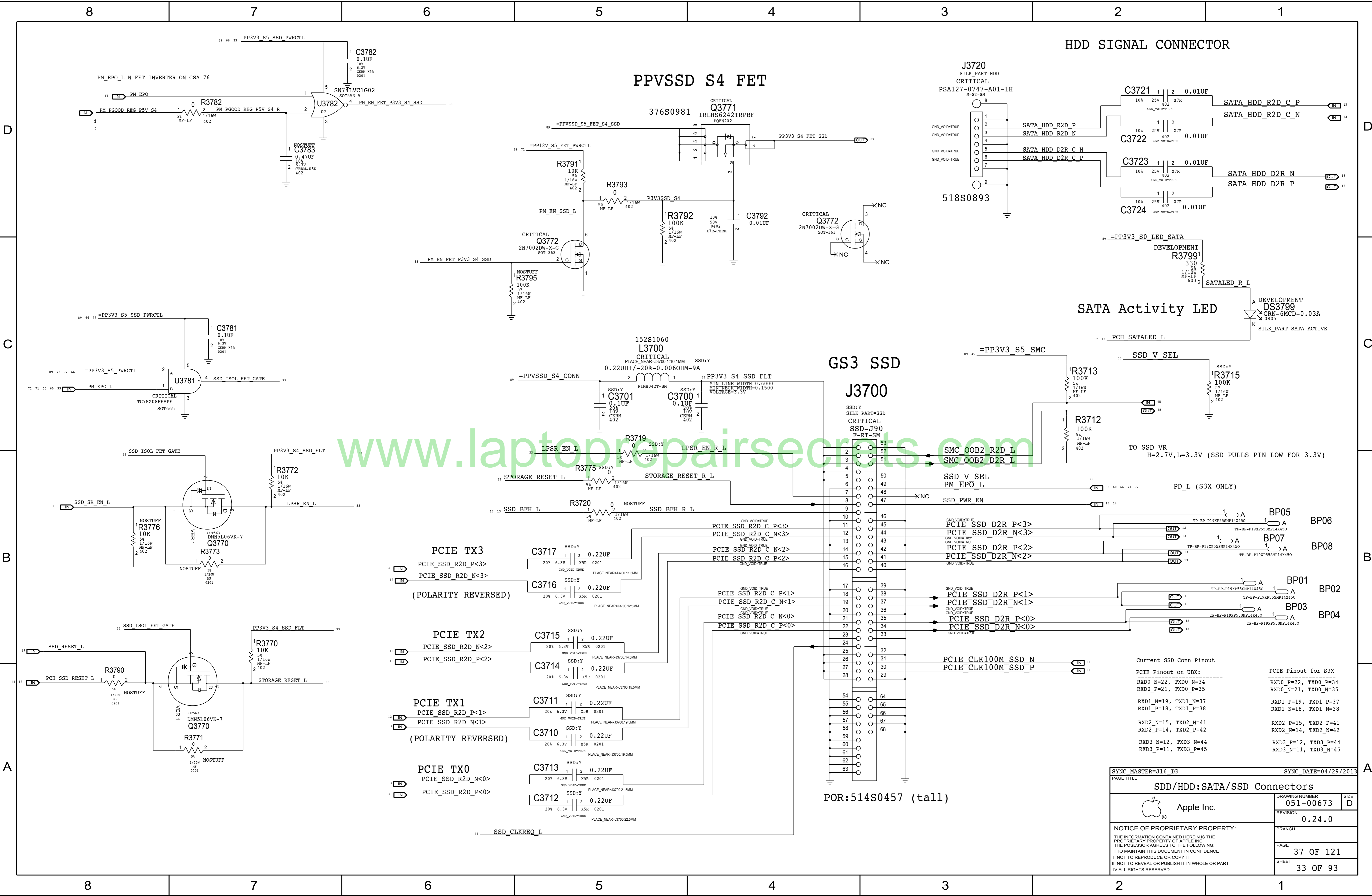
AIRPORT BLUETOOTH

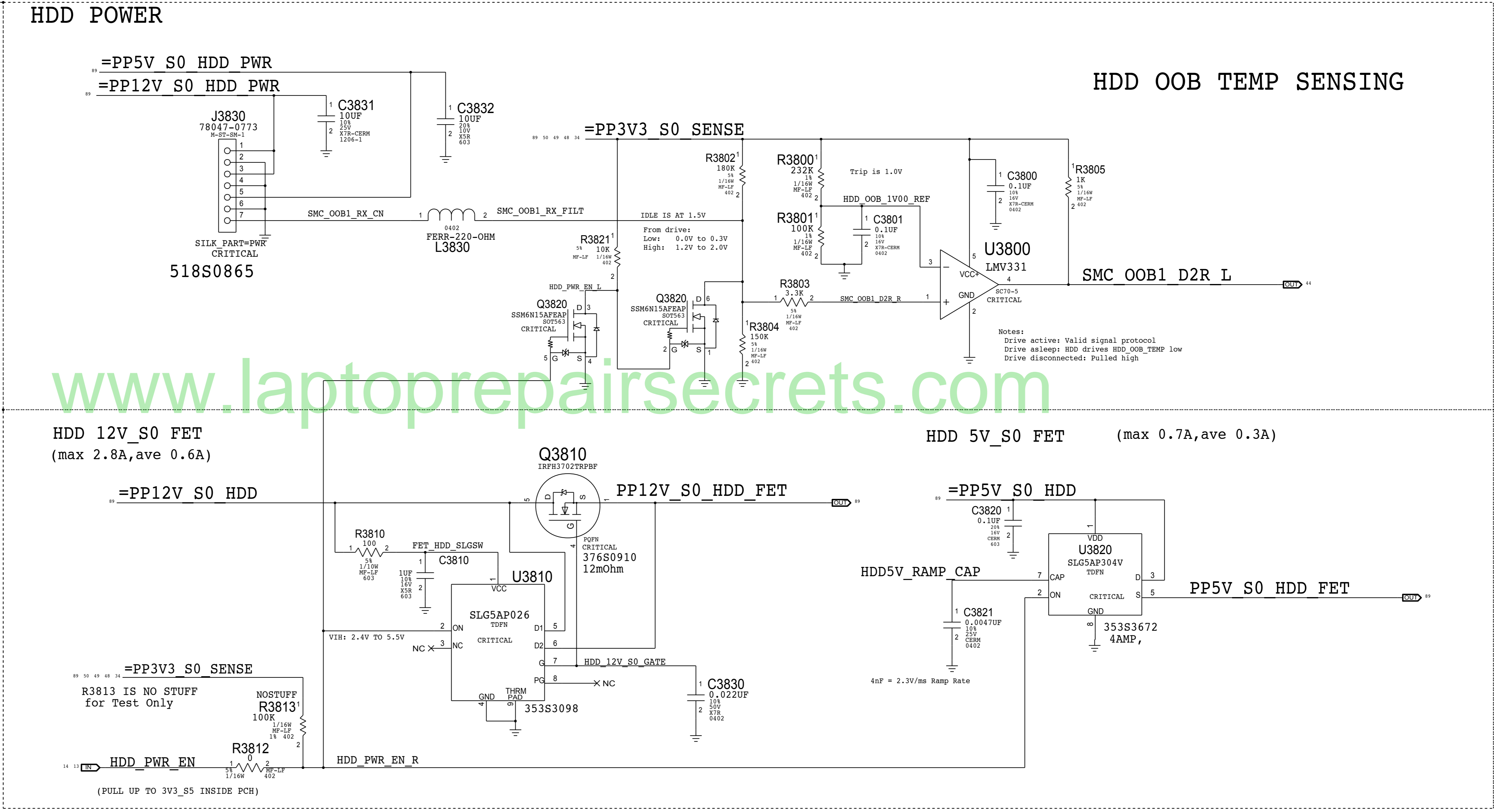


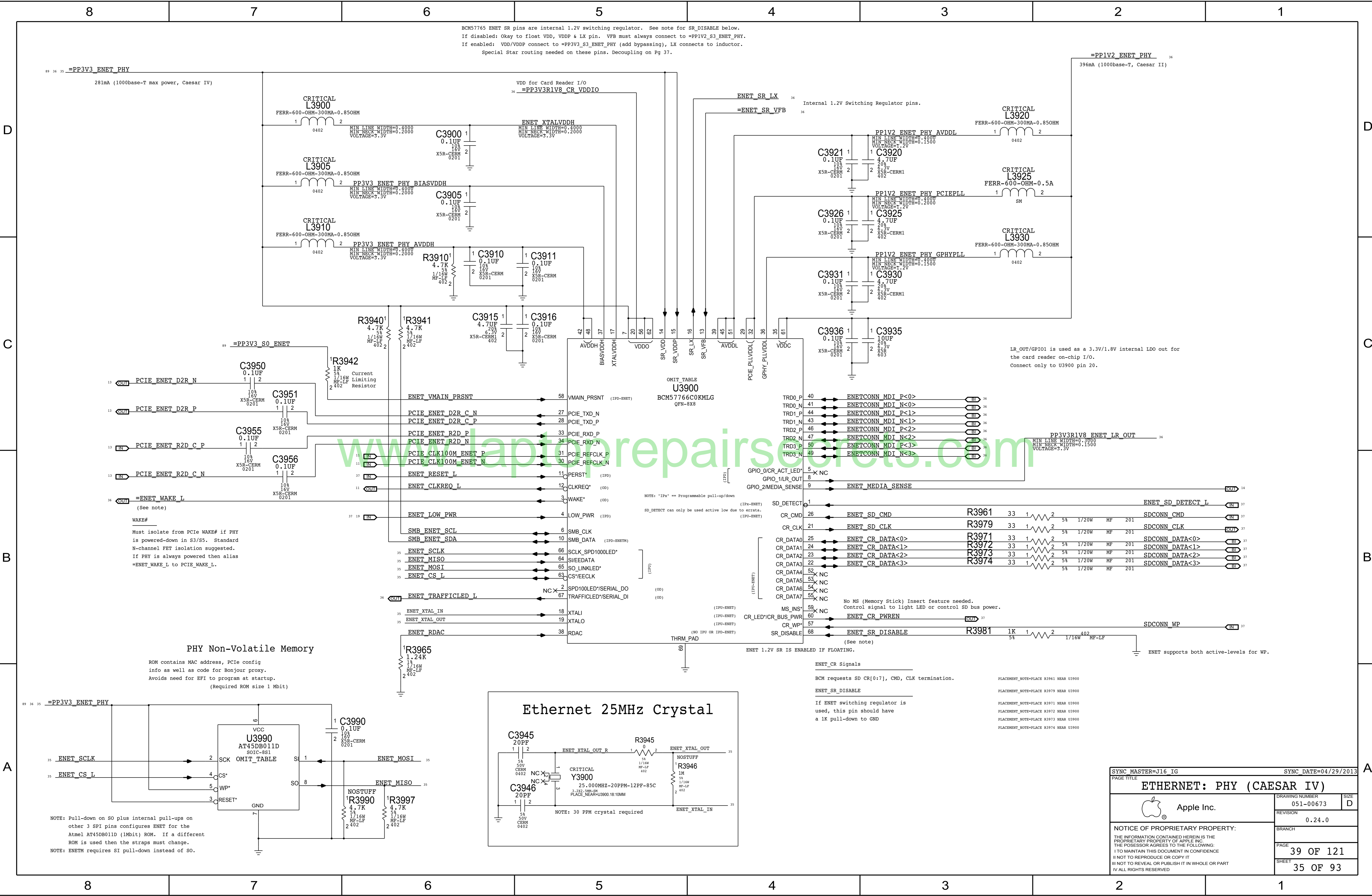
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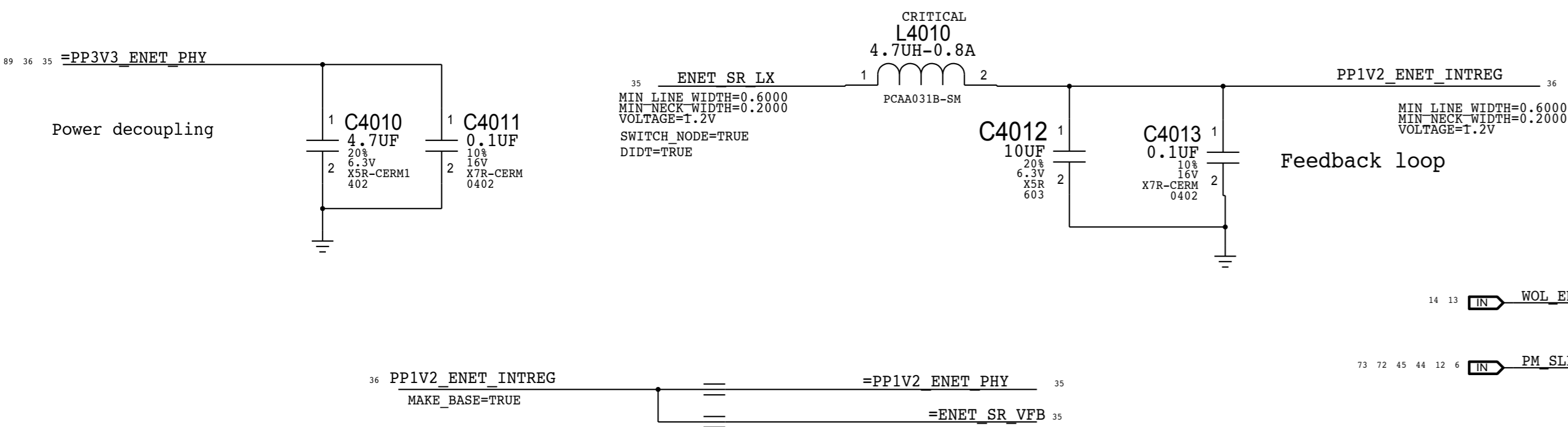
SYNC_MASTER=J16 IG		SYNC_DATE=04/29/2013	
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WIRELESS: Airport/Bluetooth			
	DRAWING NUMBER		SIZE
	051-00673		D
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	0.24.0		
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	PAGE		
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SHEET		32 OF 93	





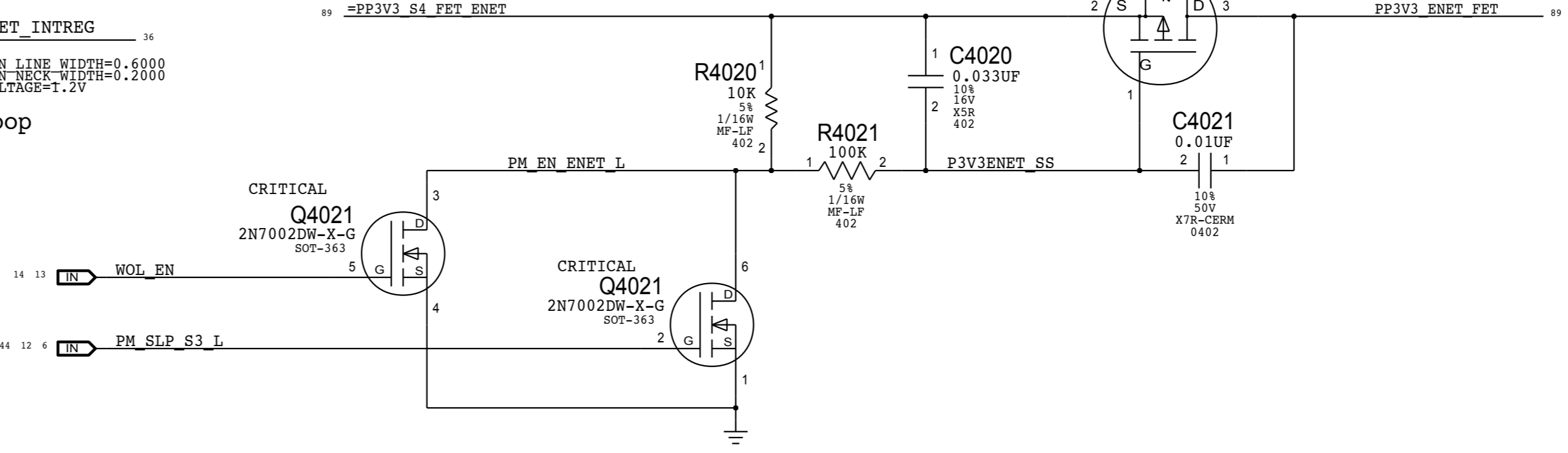


CAESAR IV 1.2V INT.VR CMPTS

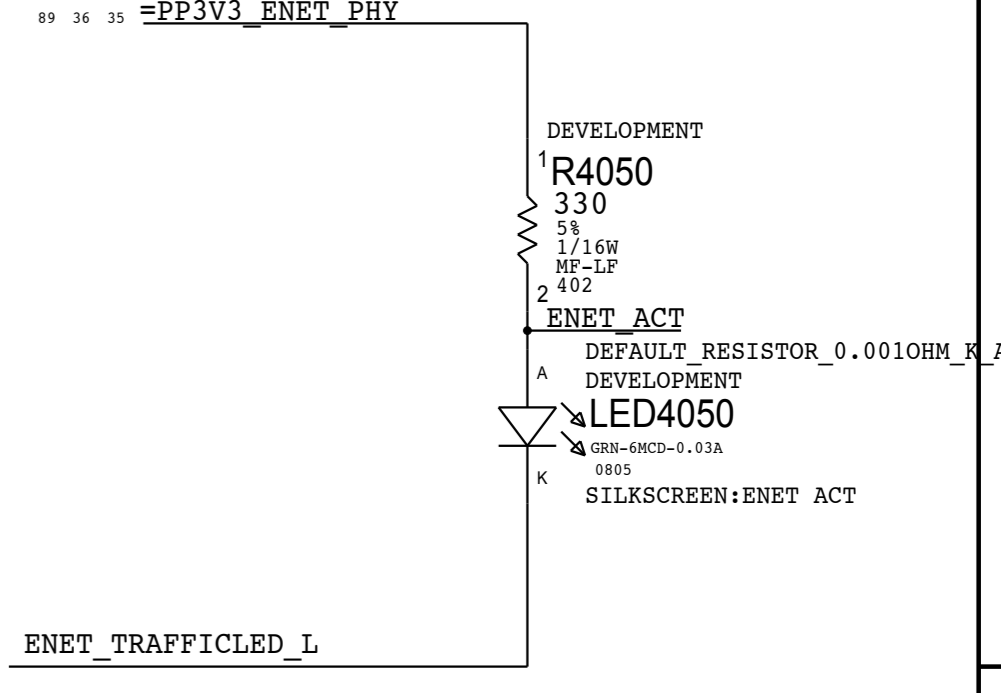


ENET Enable Generation

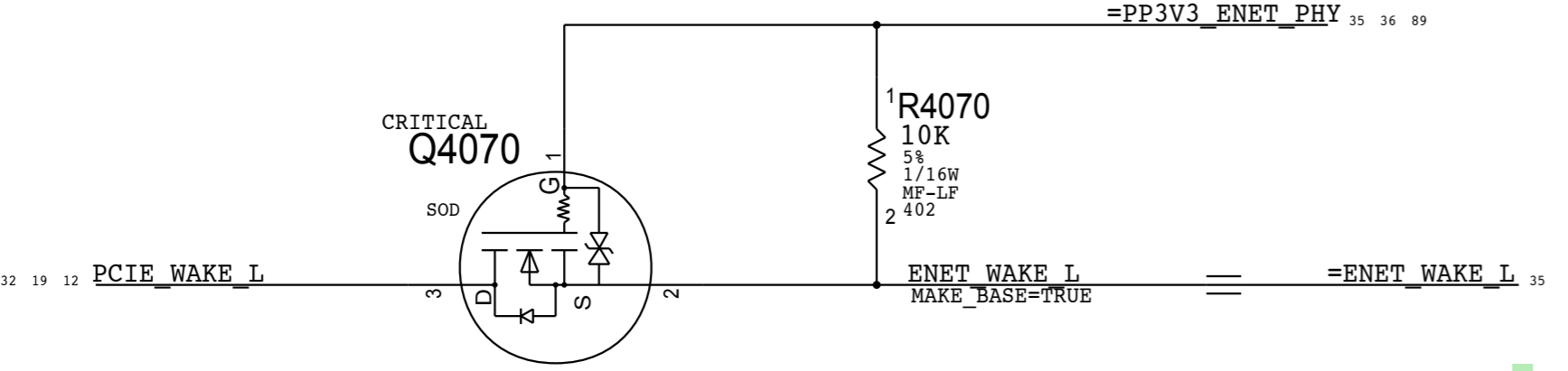
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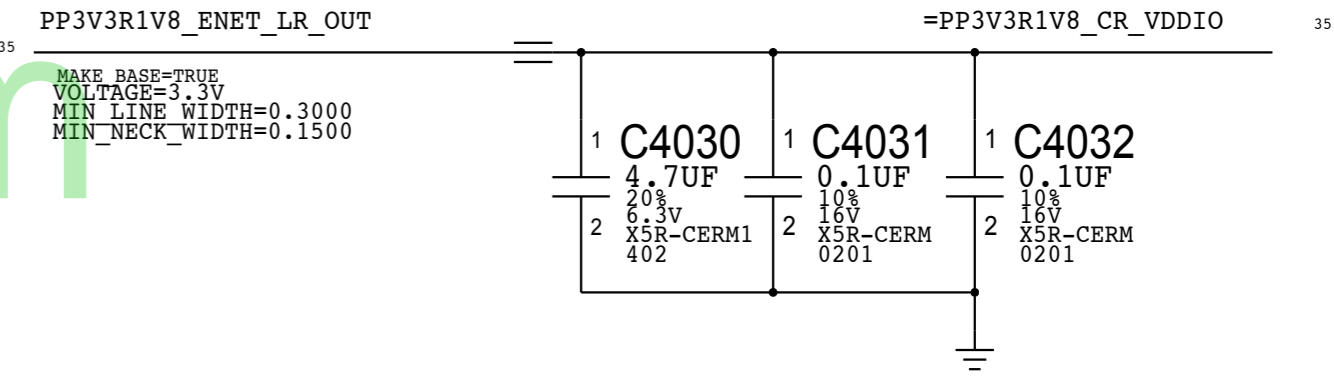
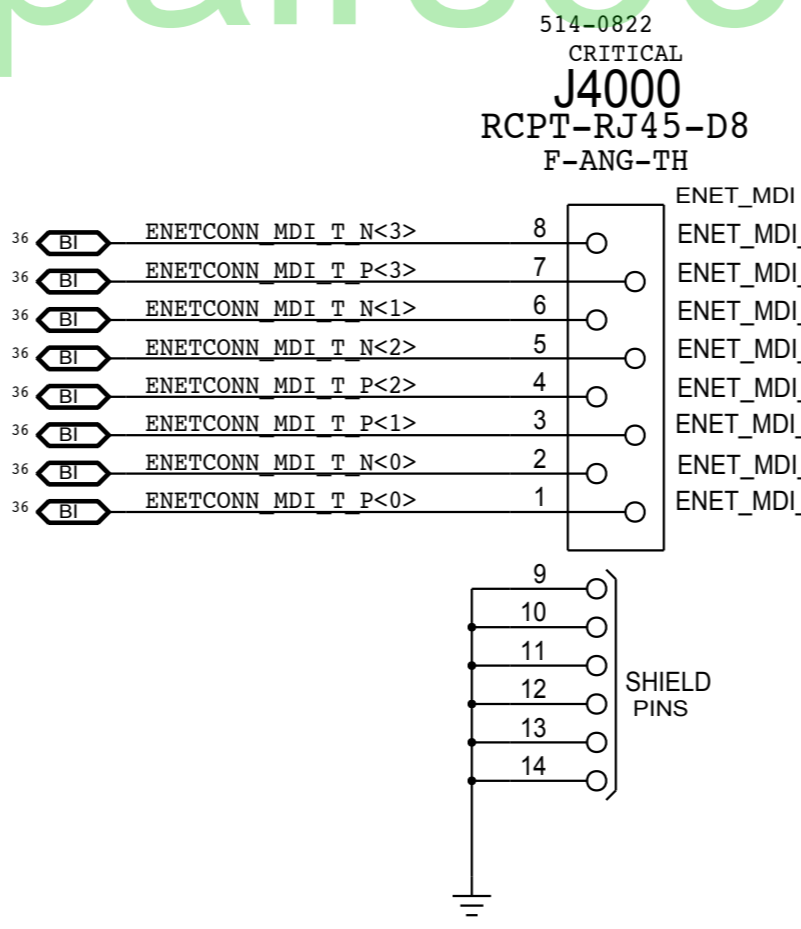
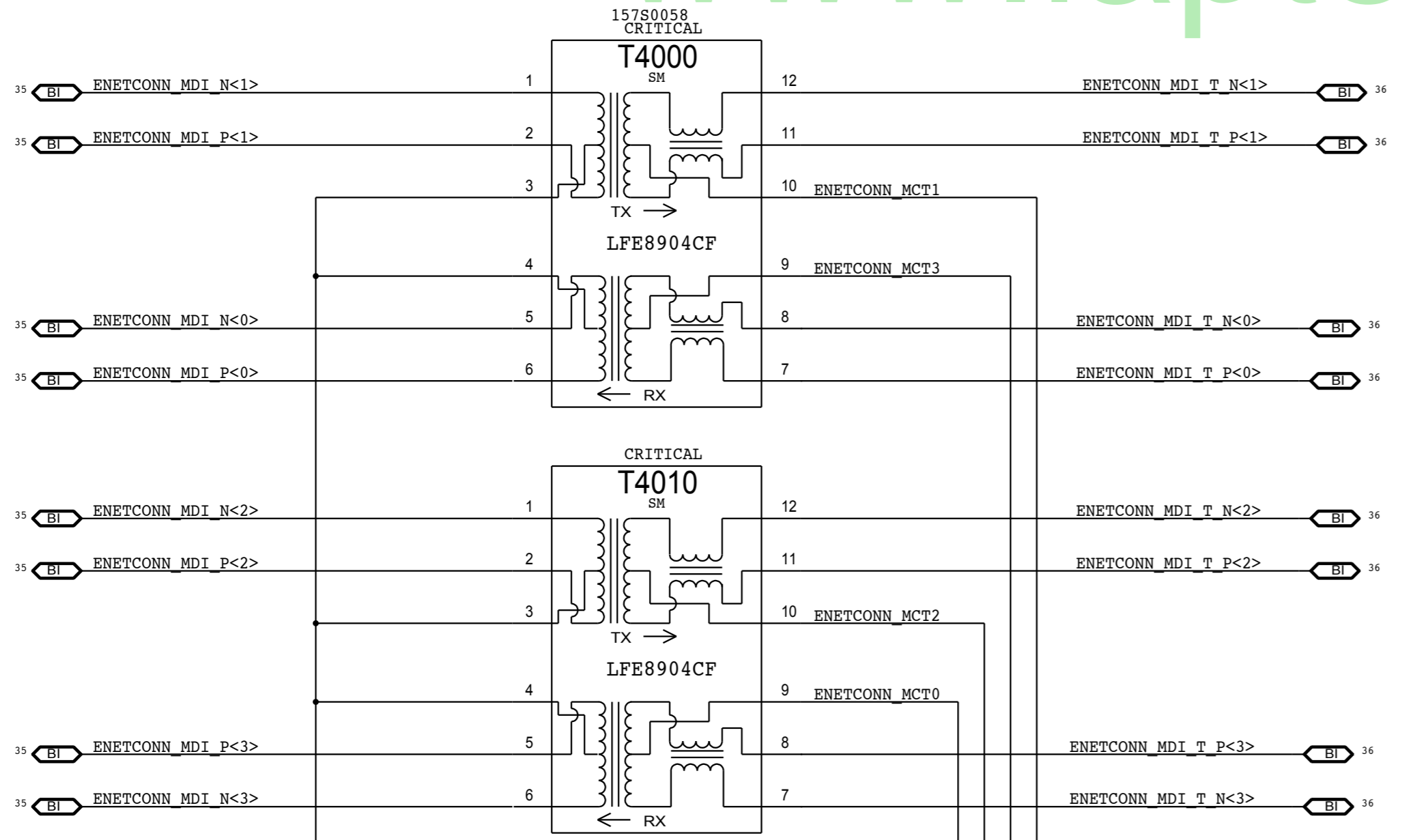
CAESAR IV ACTIVITY LED




CAESAR IV WAKE# ISOLATION



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SYNC_MASTER=J16_IG		SYNC_DATE=12/07/2012	
PAGE TITLE			
ETHERNET: Support & Connector			
 Apple Inc.	DRAWING NUMBER	051-00673	SIZE D
	REVISION 0.24.0		
	BRANCH		
NOTICE OF PROPRIETARY PROPERTY:		PAGE	
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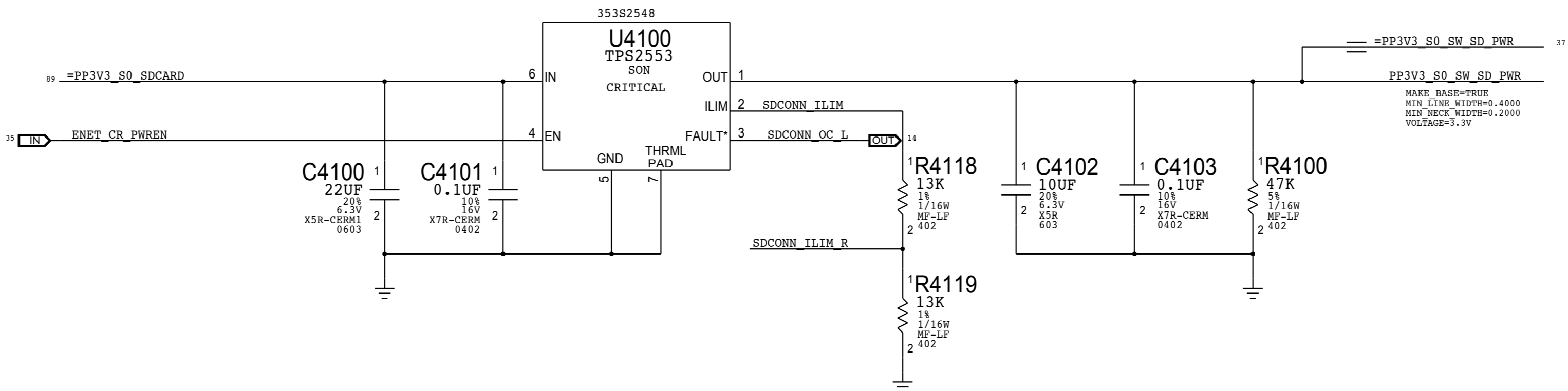
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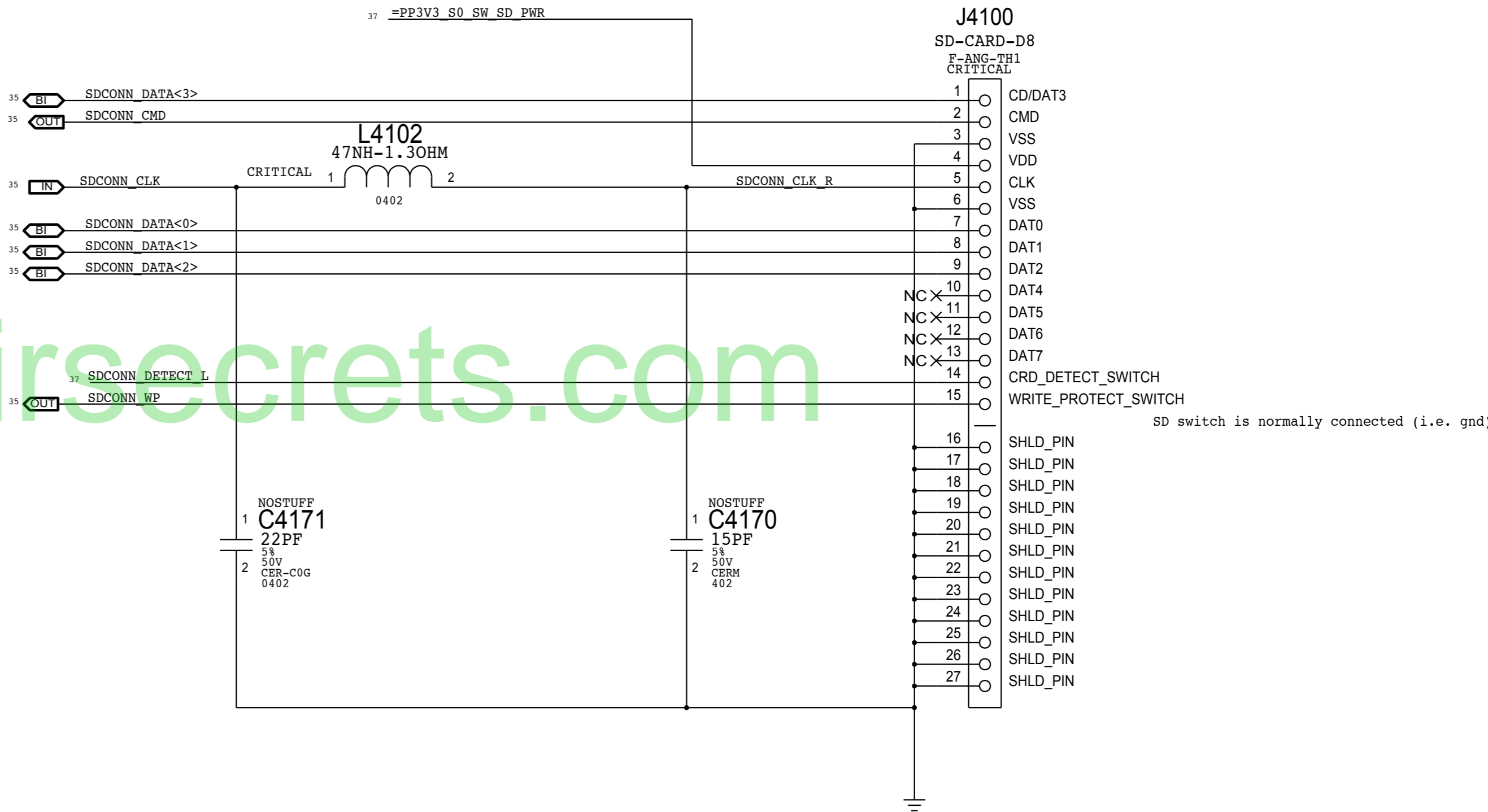
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SD CARD 3.3V OVERCURRENT PROTECTION CHIP

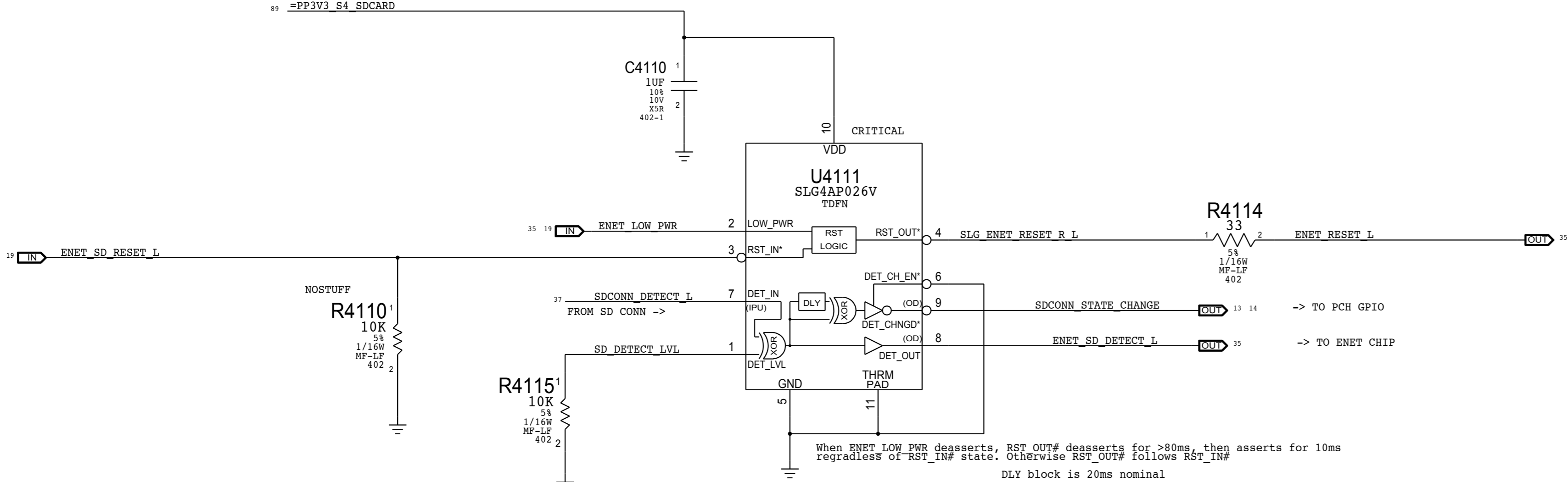


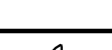
J16:516-0249 / J17:512-0038

SD CARD CONNECTOR

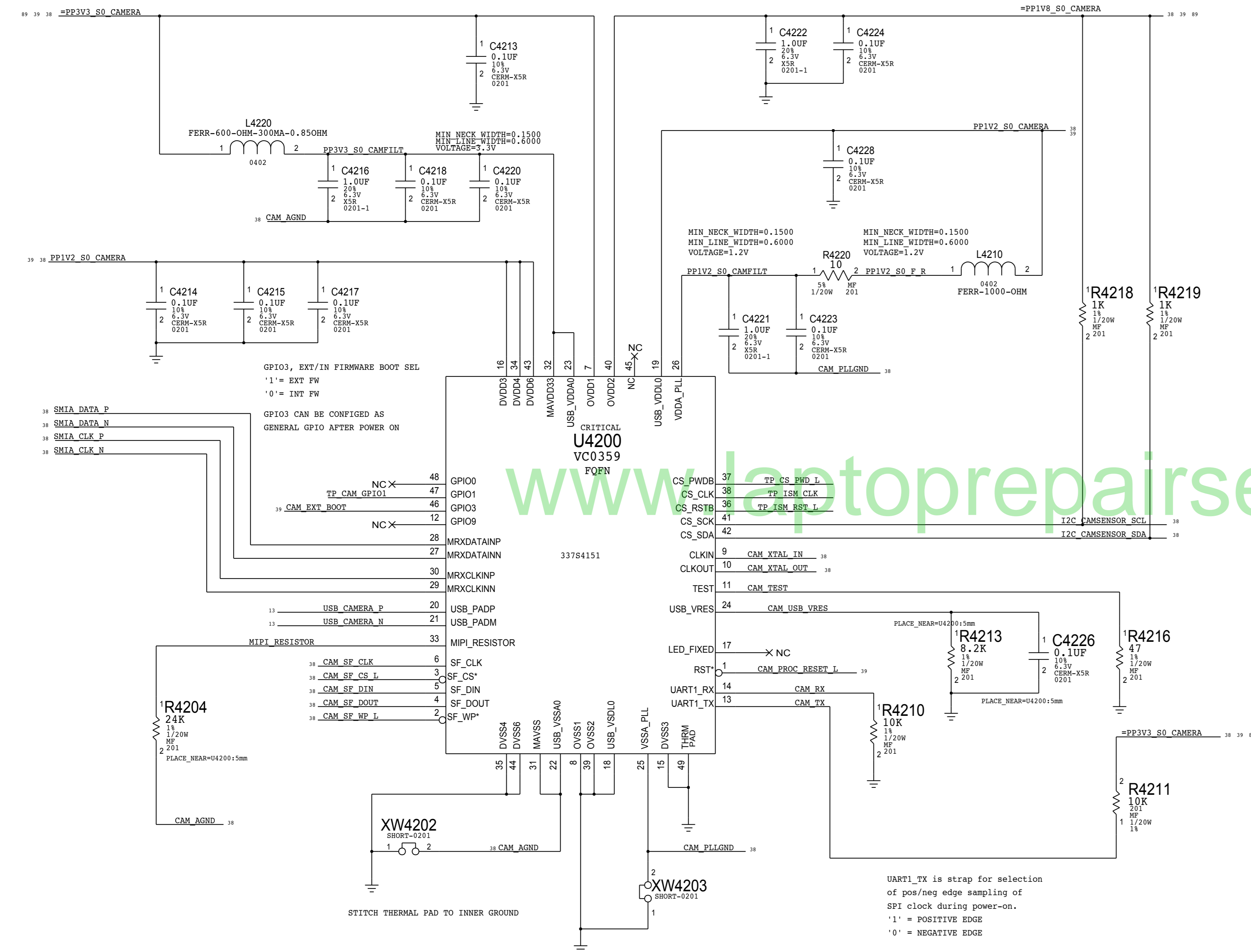


SDCONN DETECT DEBOUNCE. ENET_RESET AND DETECT-CHANGED PCH GPIO PULSE GENERATION.



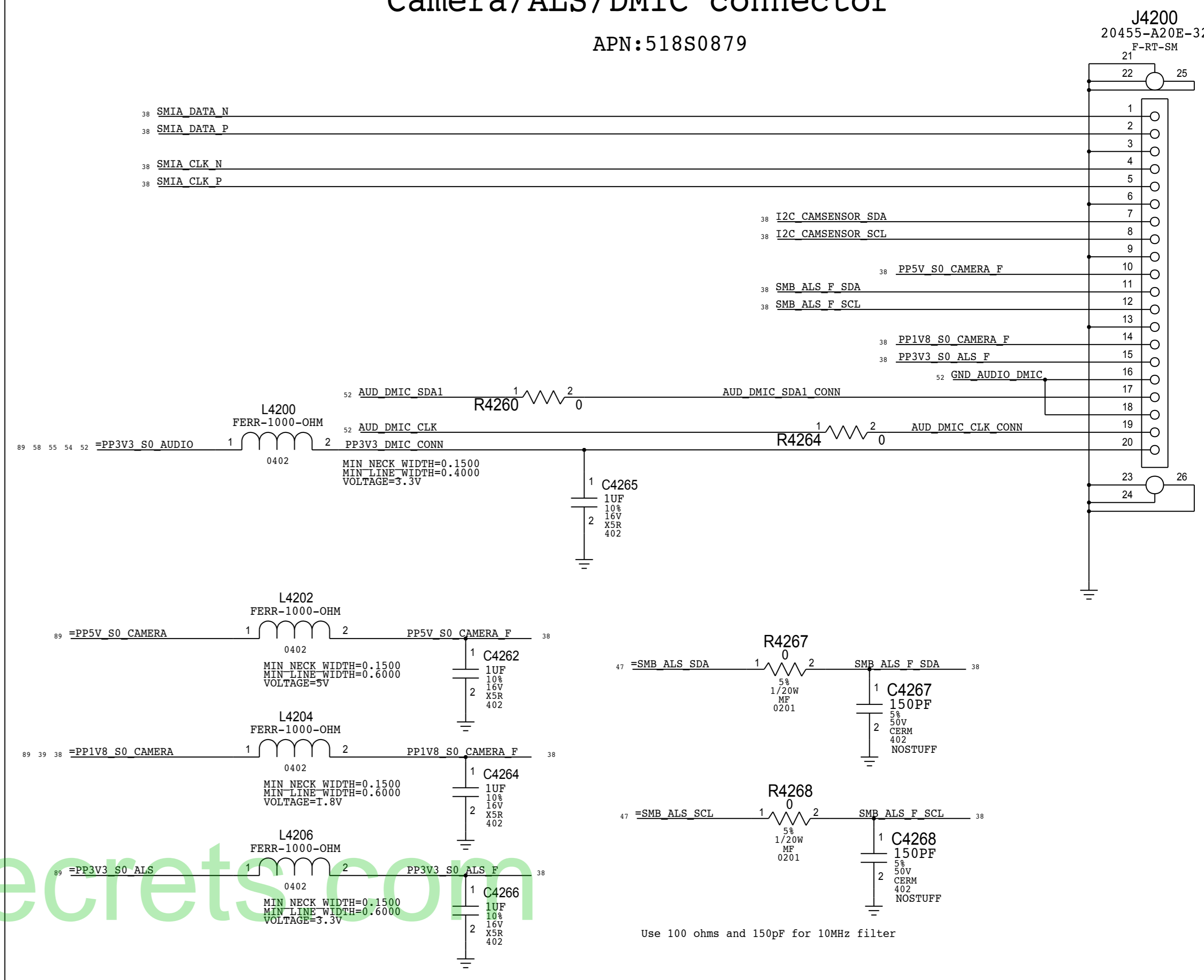
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PAGE TITLE			
SD CARD: Connector			
	Apple Inc.	DRAWING NUMBER	SIZE
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USB CAMERA CONTROLLER

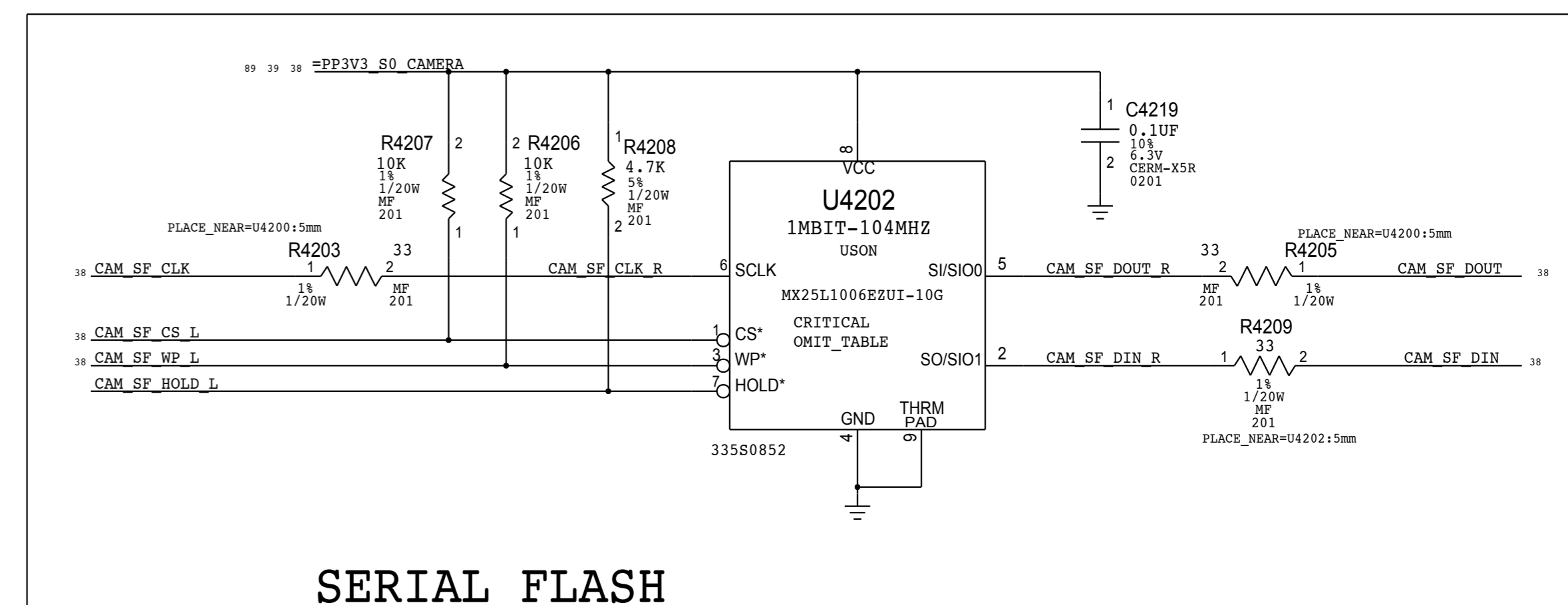


Camera/ALS/DMIC connector

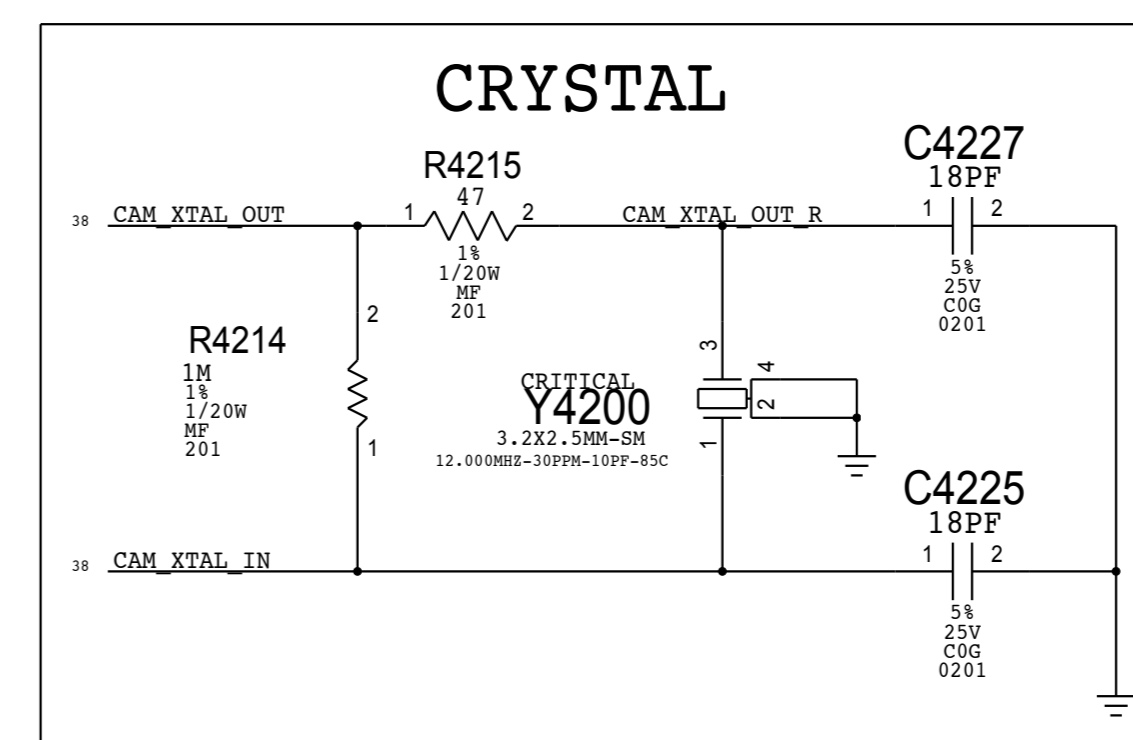
APN:518S0879




SERIAL FLASH



CRYSTAL



SYNC MASTER=J78 NAT		SYNC DATE=11/05/2013			
PAGE TITLE					
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 Apple Inc.		DRAWING NUMBER	051-00673	SIZE	D
		REVISION	0.24.0		
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		42 OF 121			
		SHEET			
		38 OF 93			

D

C

B

A

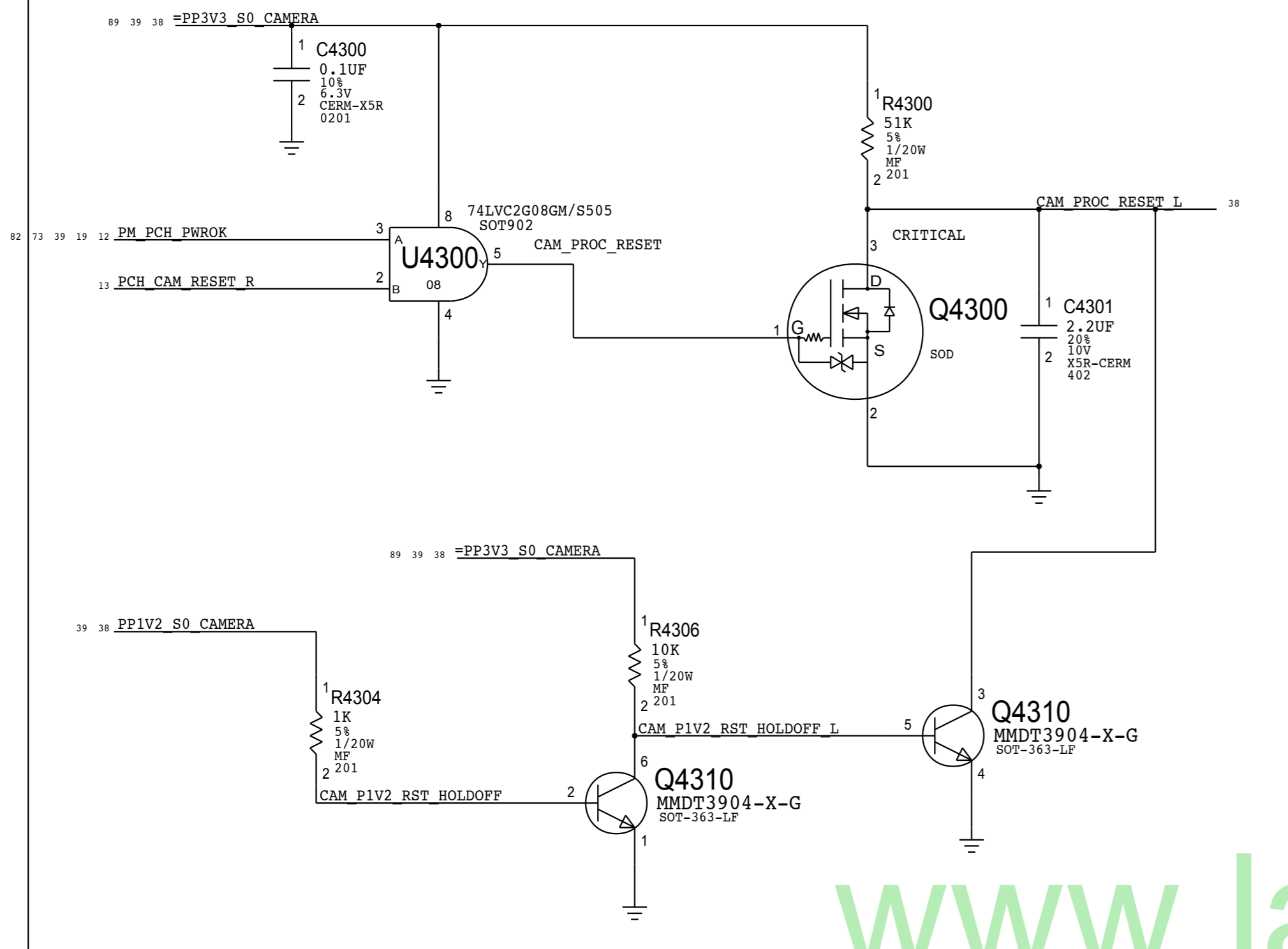
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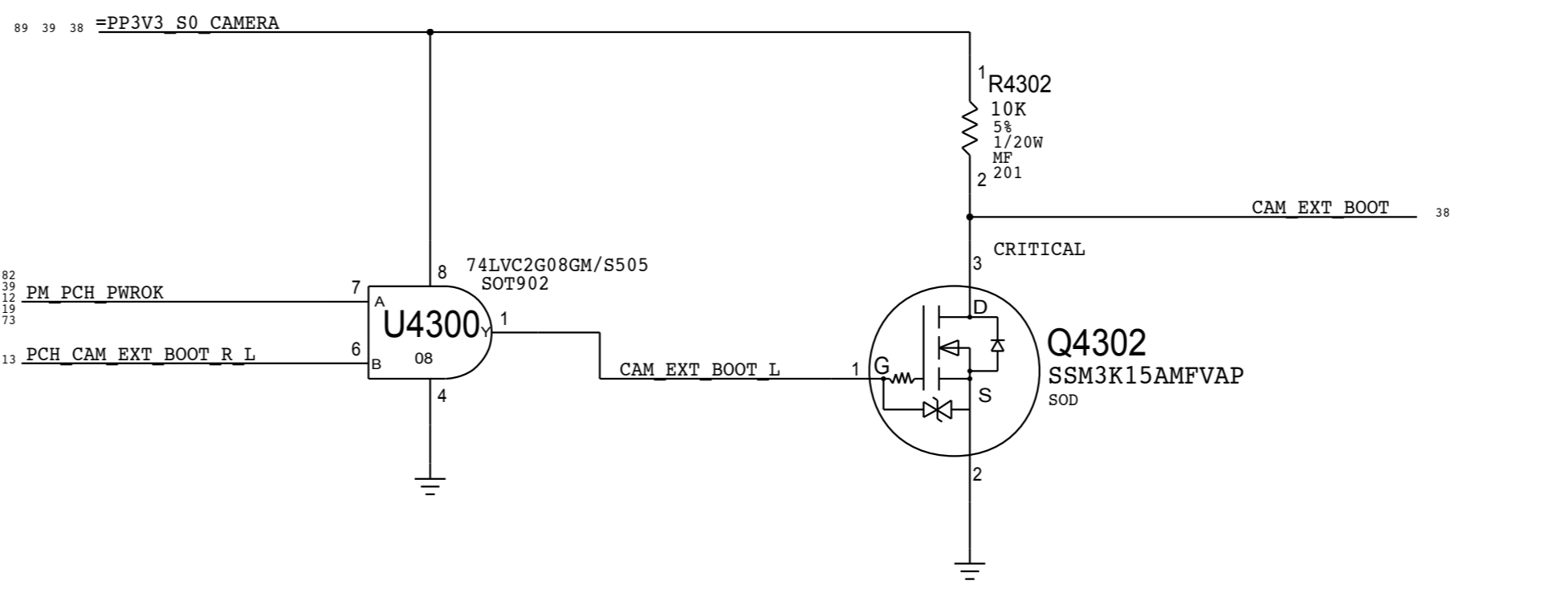
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Camera Processor Reset

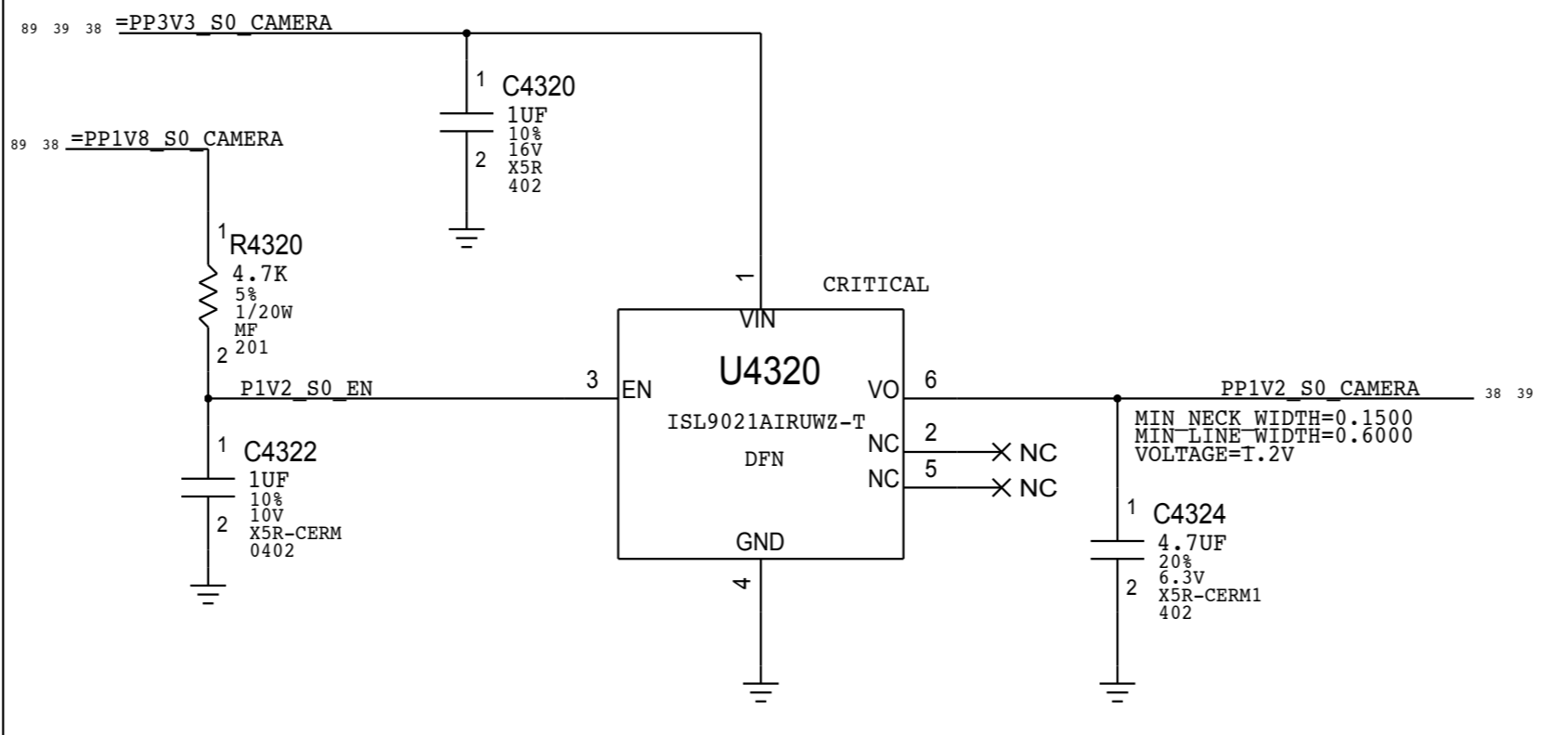



Camera Processor ExtBoot Cntl



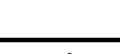
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PP1V2_S0_CAMERA VREG



SYNC MASTER=J78 NAT		SYNC DATE=11/05/2013	
PAGE TITLE			
CAMERA: Controller Support			
	DRAWING NUMBER		SIZE
	051-00673		D
REVISION		0.24.0	
BRANCH			
PAGE		43 OF 121	
SHEET		39 OF 93	
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SYNC MASTER=J78 KENNY		SYNC DATE=10/09/2013	
PAGE TITLE			
DISPLAY: MUXing			
 Apple Inc.	DRAWING NUMBER		SIZE
	051-00673		D
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		BRANCH	
		PAGE	45 OF 121
		SHEET	41 OF 93

D

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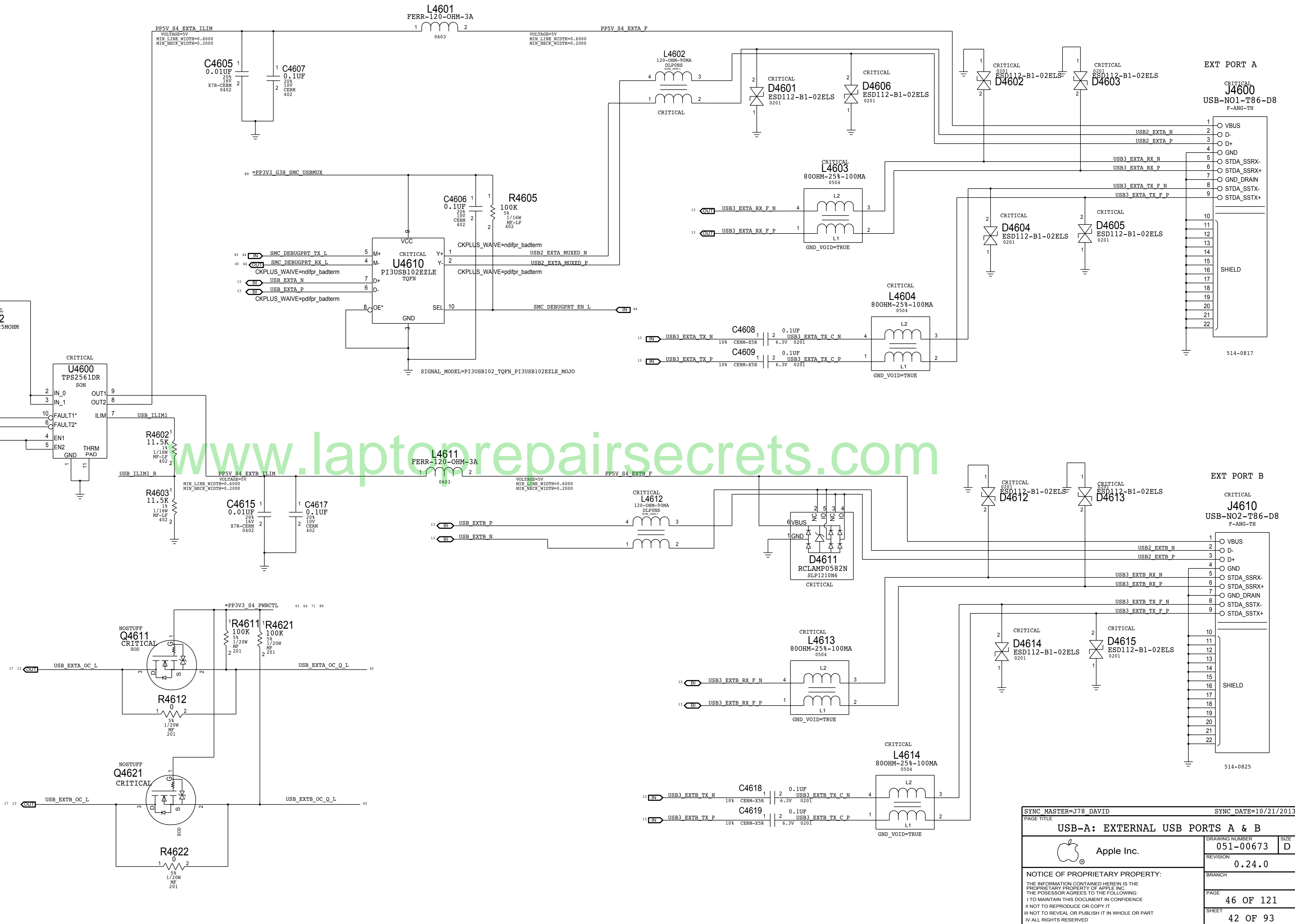
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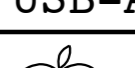
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SYNC_MASTER=J78 DAVID		SYNC_DATE=10/21/2013	
PAGE TITLE			
USB-A: EXTERNAL USB PORTS A & B			
 Apple Inc.		DRAWING NUMBER	SIZE
		051-00673	D
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		BRANCH	
		PAGE	46 OF 121
		SHEET	42 OF 93

D

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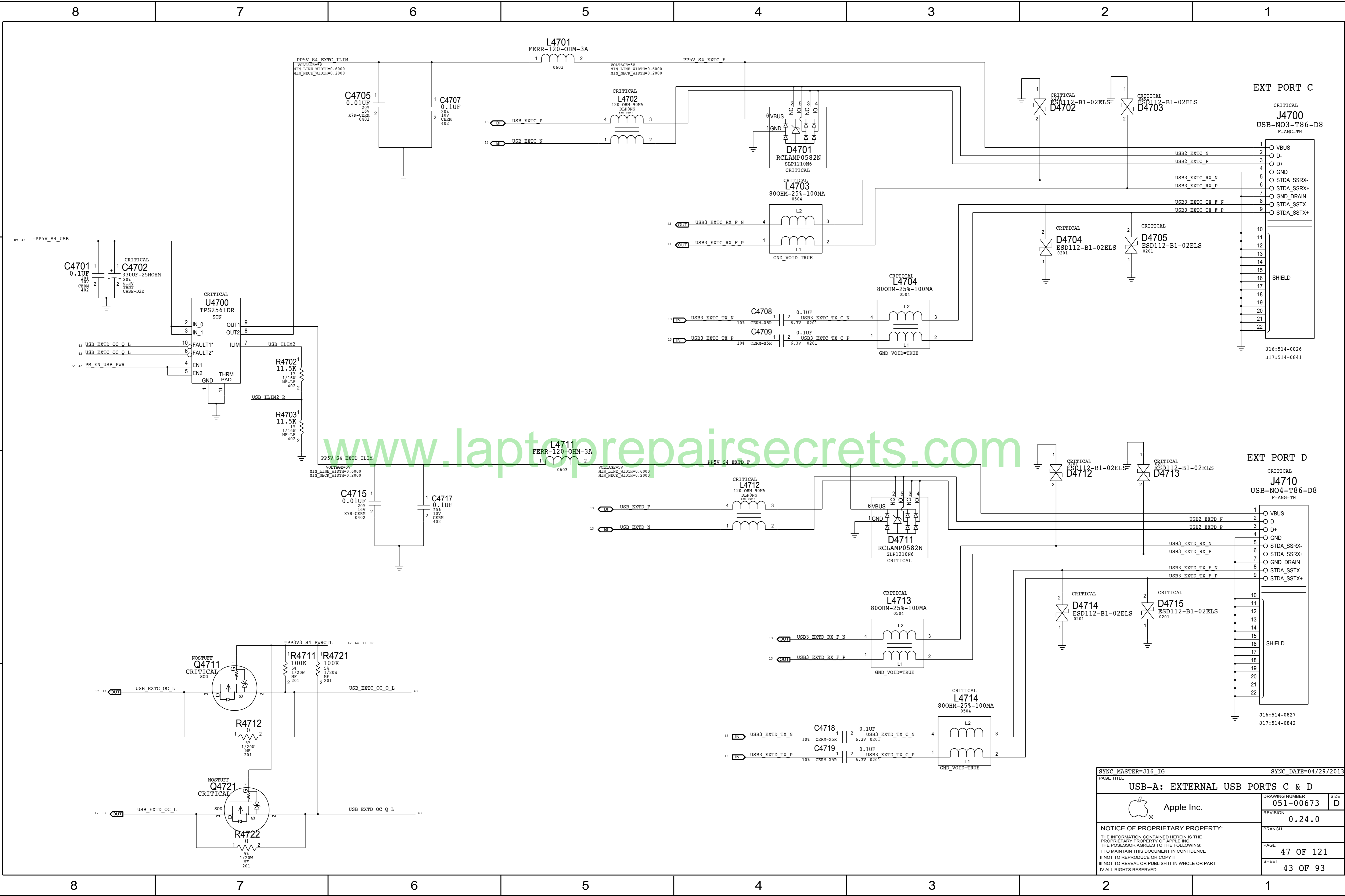
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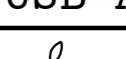
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PAGE TITLE			
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	DRAWING NUMBER		SIZE
	051-00673		D
Apple Inc.	REVISION		
	0.24.0		
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		47 OF 121	
		SHEET	
	43 OF 93		

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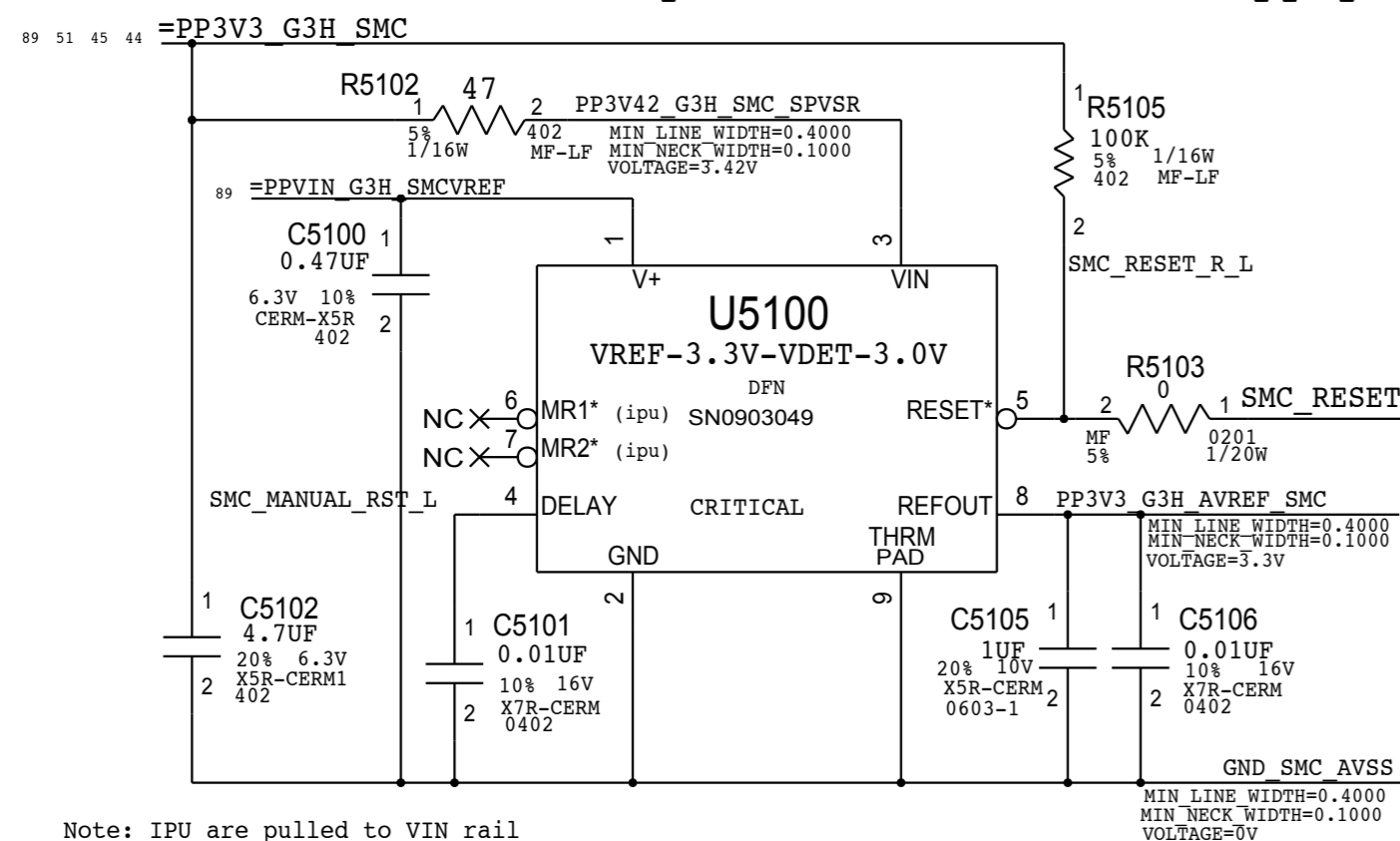
D

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SMC Supervisor and AVREF Supply



Note: IPU are pulled to VIN rail

ADC Channel Aliases

SMC_ADC0	VSNS P12VG3H	VD2R
SMC_ADC1	VSNS P12VG3H	ID2R
SMC_ADC2	VSNS P12VS0 CPUCORE	VD20
SMC_ADC3	VSNS P12VS0 CPUCORE	ID20
SMC_ADC4	VSNS CPUVCC	VC0C
SMC_ADC5	VSNS CPUVCC	IC0C
SMC_ADC6	VSNS CPUVCC GT	VC0G
SMC_ADC7	VSNS CPUVCC GT	IC0G
SMC_ADC8	VSNS CPUVCC IO	IC0I
SMC_ADC9	VSNS P1V35S0	IC0M
SMC_ADC10	VSNS CPUVCC SA	IC0S
SMC_ADC11	VSNS P12VS0 FBVDDQ	IG1F
SMC_ADC12	VSNS GPUCORE ALT	VG0C
SMC_ADC13	VSNS GPU CORE ALT	IG0C
SMC_ADC14	VSNS GPU VDDCI	VG0I
SMC_ADC15	VSNS GPU VDDCI	IG0I
SMC_ADC16	VSNS P12VS0 GPU AUX	IG1A
SMC_ADC17	VSNS P12VS0 GPU CORE	IG1C
SMC_ADC18	VSNS P12VS0 HDD	IH02
SMC_ADC19	VSNS HDDS0	IH05
SMC_ADC20	VSNS SSD S4	VH1R
SMC_ADC21	VSNS SSD S4	IH1R
SMC_ADC22	VSNS VDDQ3 DDR	VM0R
SMC_ADC23	VSNS VDDQ3 DDR	IM0R

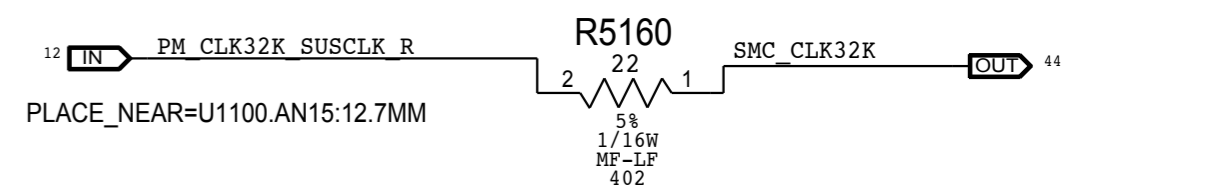
Project-specific Aliases

SMC_PN5	ACDC BURST EN L	VD2R
SMC_PJ3	SMC OOB2 R2D L	33
SMC_PJ2	SMC OOB2 D2R L	33
SMC_PP0	SMC ACDC ID	60
SMC_PH2	SMC ASSERT RTCRST	18 45
SMC_PL6	SMC WIT1 PWR EN	45
SMC_PN3	TCON BLC EN (LED-4)	80 (100K PD AT BLC)
SMC_PH7	GPY OK L (LED-3)	3 80 (5K PU AT MLB)
SMC_PN7	DP LINK OK (LED-3)	3 80

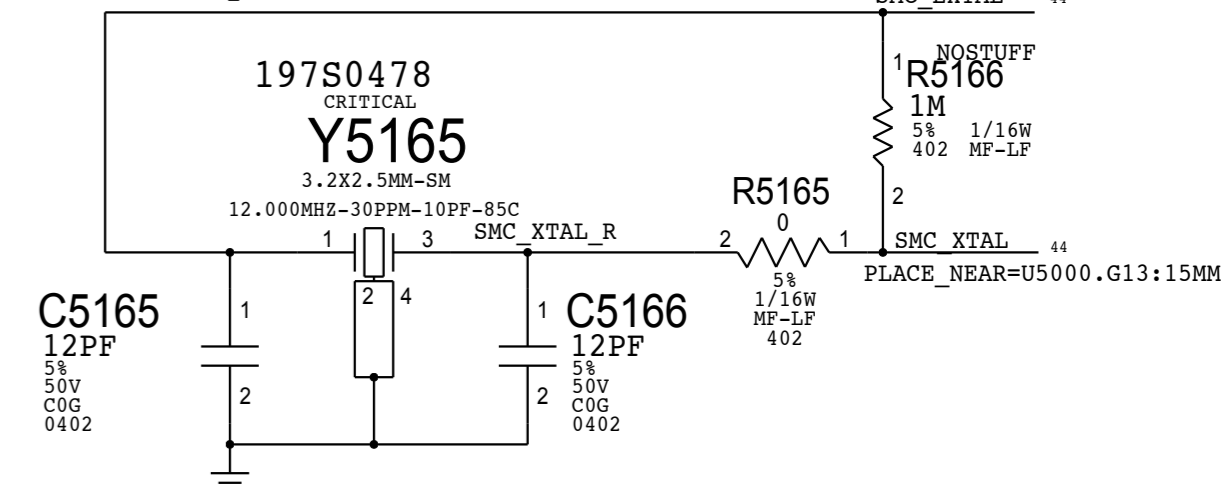
Unused Project-specific

SMC_PP0	NC SMC PF0	
SMC_PP1	NC SMC PF1	
SMC_PP2	NC SMC PF2	
SMC_PP3	NC SMC PF3	
SMC_PL7	SMC BT PWR EN (J95 new)	32 45
SMC_PP4	NC SMC S4 WAKESRC EN	
SMC_PP5	NC SMC PP5	
SMC_PP6	NC SMC PP6	
SMC_PP7	NC SMC PP7	
SMC_DP_HPD_L	NC SMC DP HPD L	
SMC_PME_S4_DARK_L	NC SMC PME S4 DARK L	
SMC_PC4	NC SMC S5 PWRGD VIN	
SMC_PQ3	NC G3 POWERON L	
SMC_PN6	NC SMC G3 WAKESRC EN	
SMBUS_SMC_4_ASF_SCL	NC SMBUS_SMC_4_ASF_SCL	
SMBUS_SMC_4_ASF_SDA	NC SMBUS_SMC_4_ASF_SDA	
SMBUS_SMC_5_G3H_SCL	NC SMBUS_SMC_5_G3H_SCL	
SMBUS_SMC_5_G3H_SDA	NC SMBUS_SMC_5_G3H_SDA	
SMC_OOB1_R2D_L	NC SMC OOB1 R2D L	
SMC_BATLOW_L	NC SMC_SMC_BATLOW_L	
SMC_PH3	NC SMC_PH3	

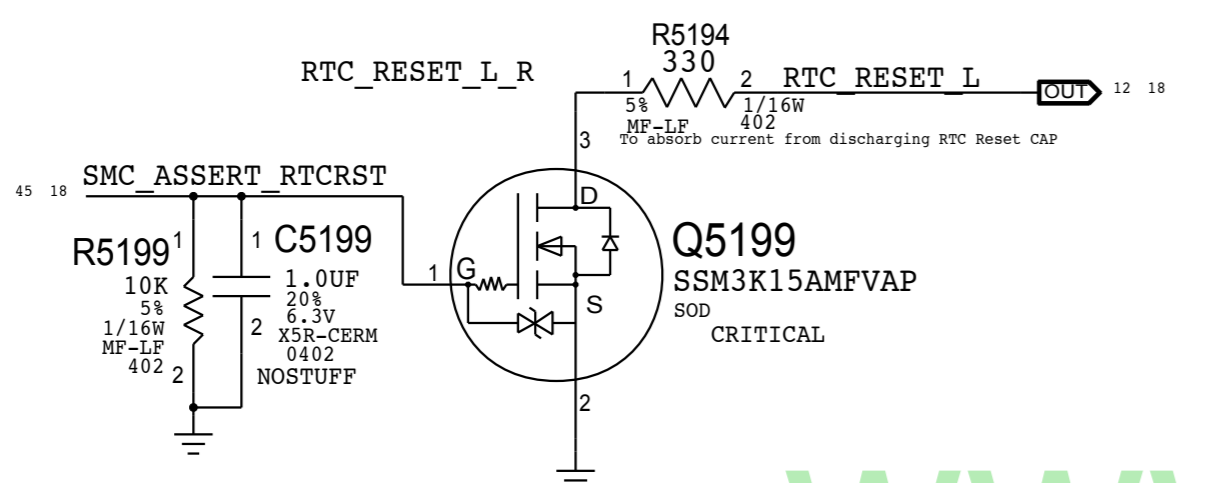
SMC 32KHz Clock



SMC Crystal



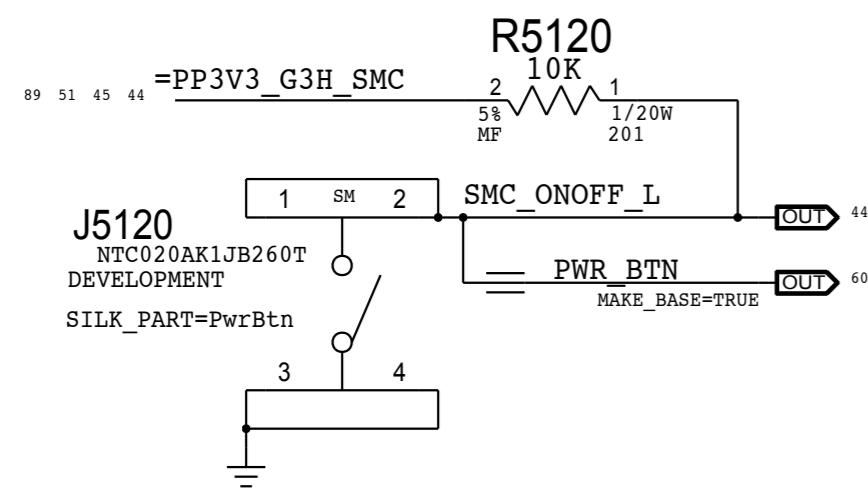
SMC Controlled RTC Reset



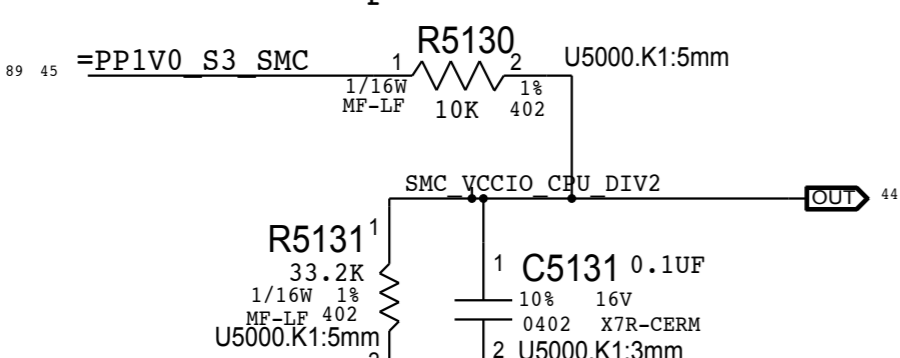
PECI Support

Level-shifter that allows SMC to drive Peci. Place this circuit near the Tee point to minimize reflections.

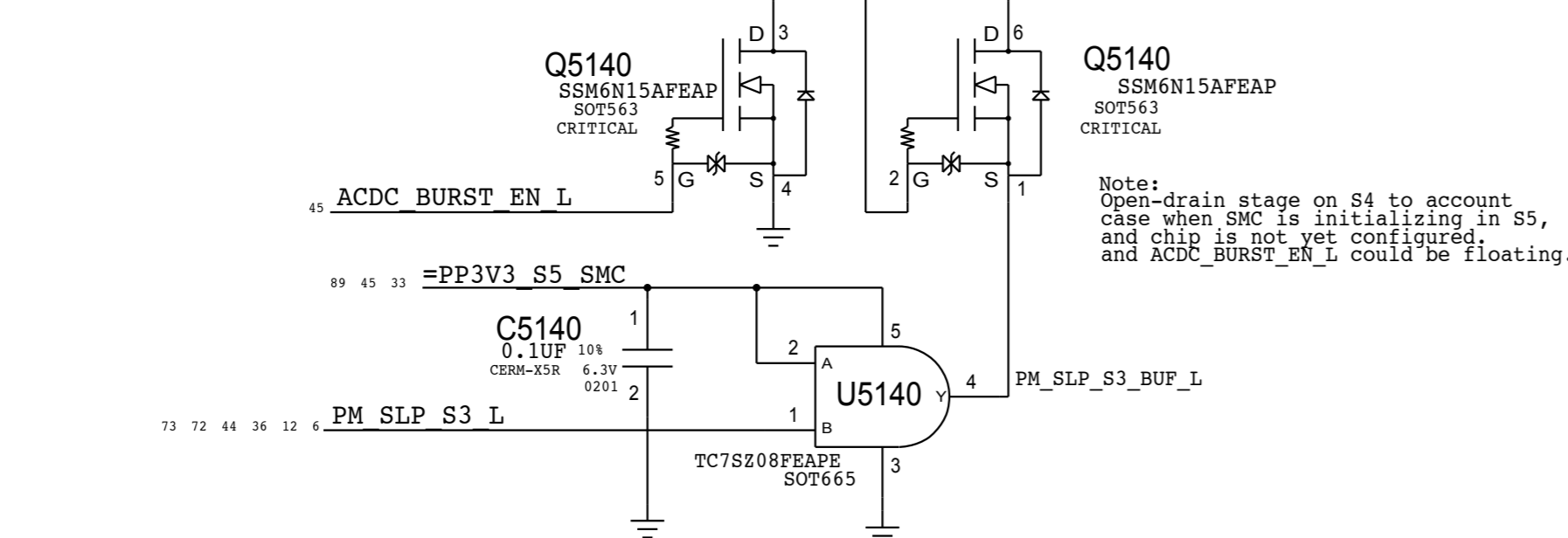
Power Button



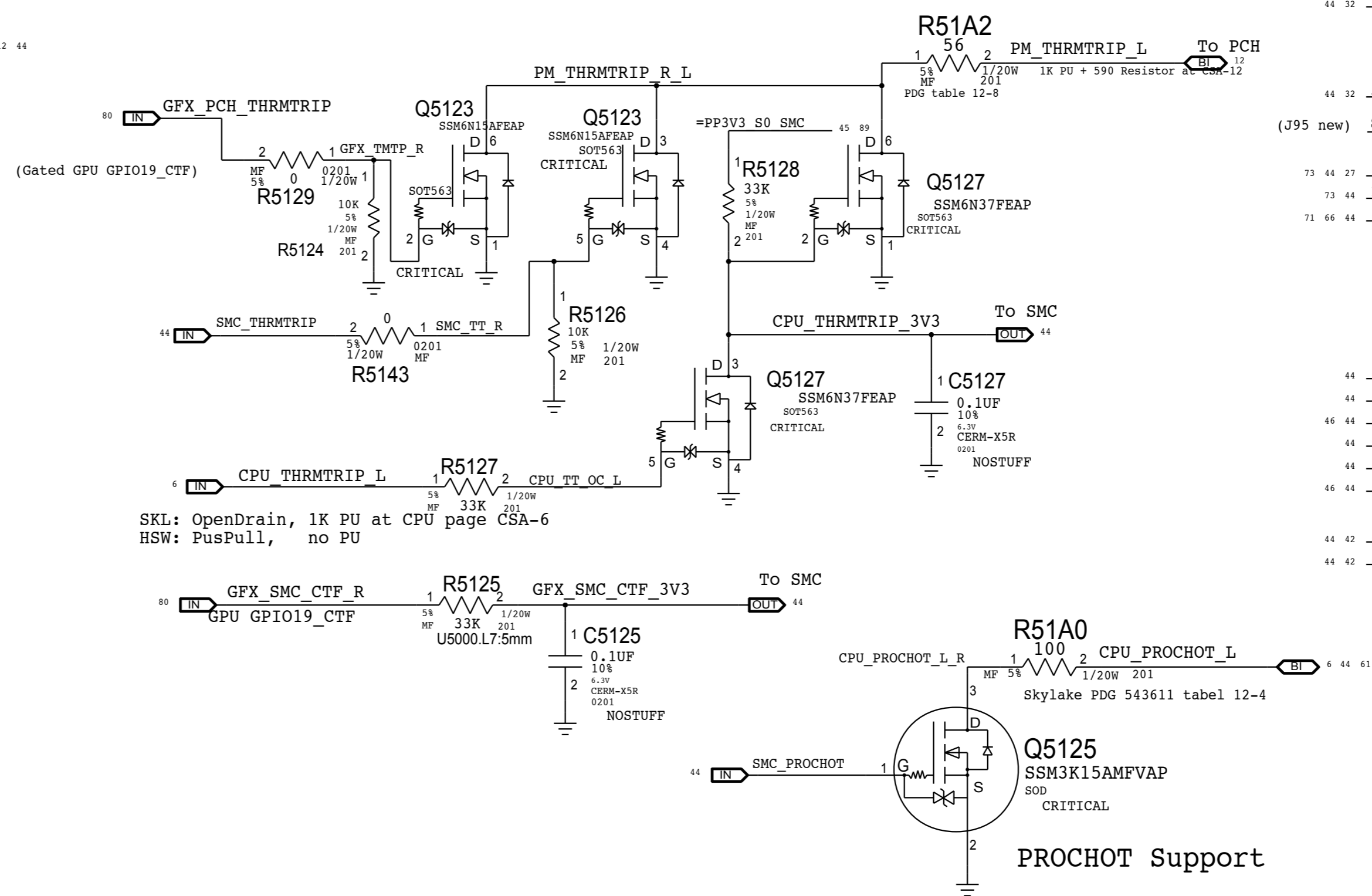
Comparator VRef



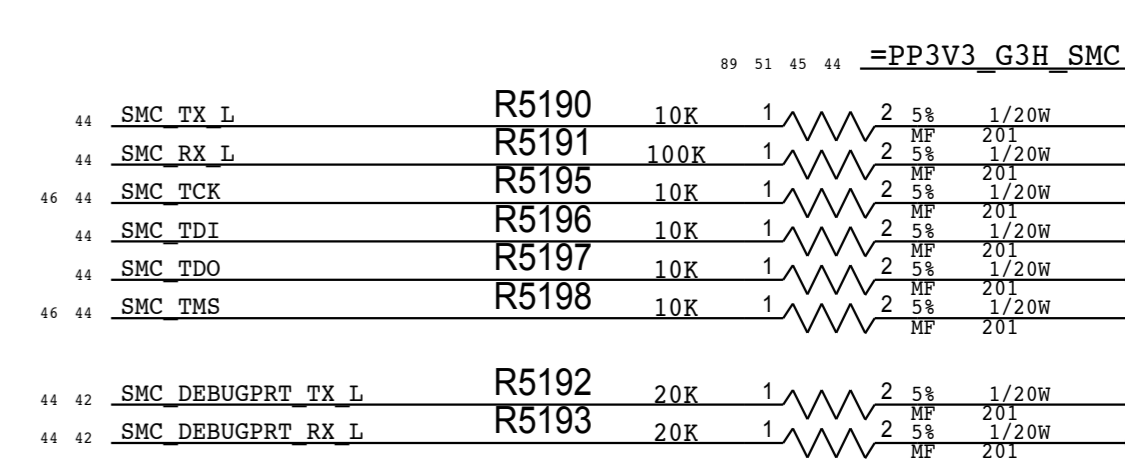
AC/DC Burst Mode Enable



Platform Thermal Control



Serial/JTAG Interface Pull-ups



SYNC_MASTER=BRANCH JERRYCHOW		SYNC_DATE=11/06/2014	
PAGE TITLE			
SMC: Controller Support		DRAWING NUMBER	051-00673
Apple Inc.		REVISION	0.24.0
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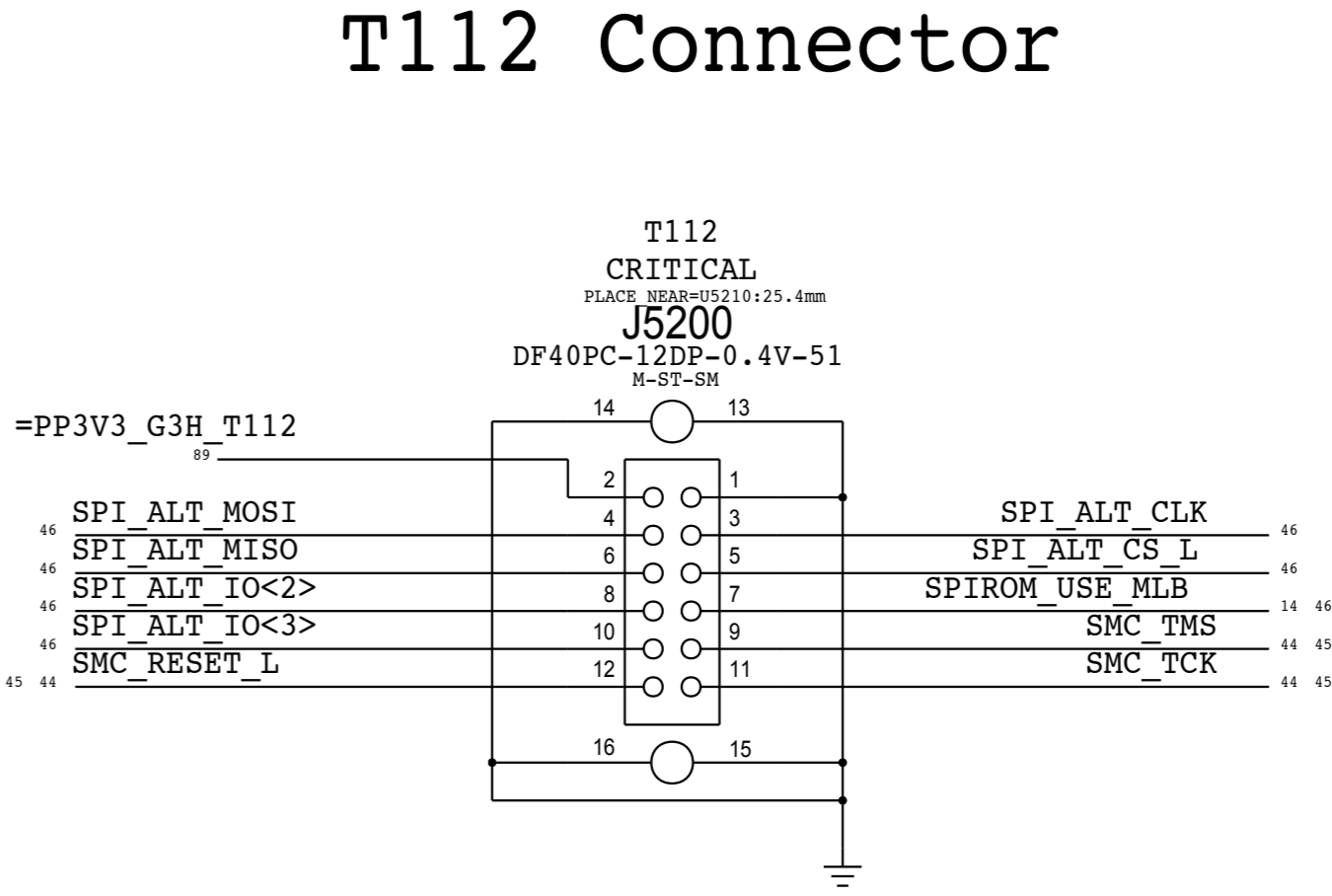
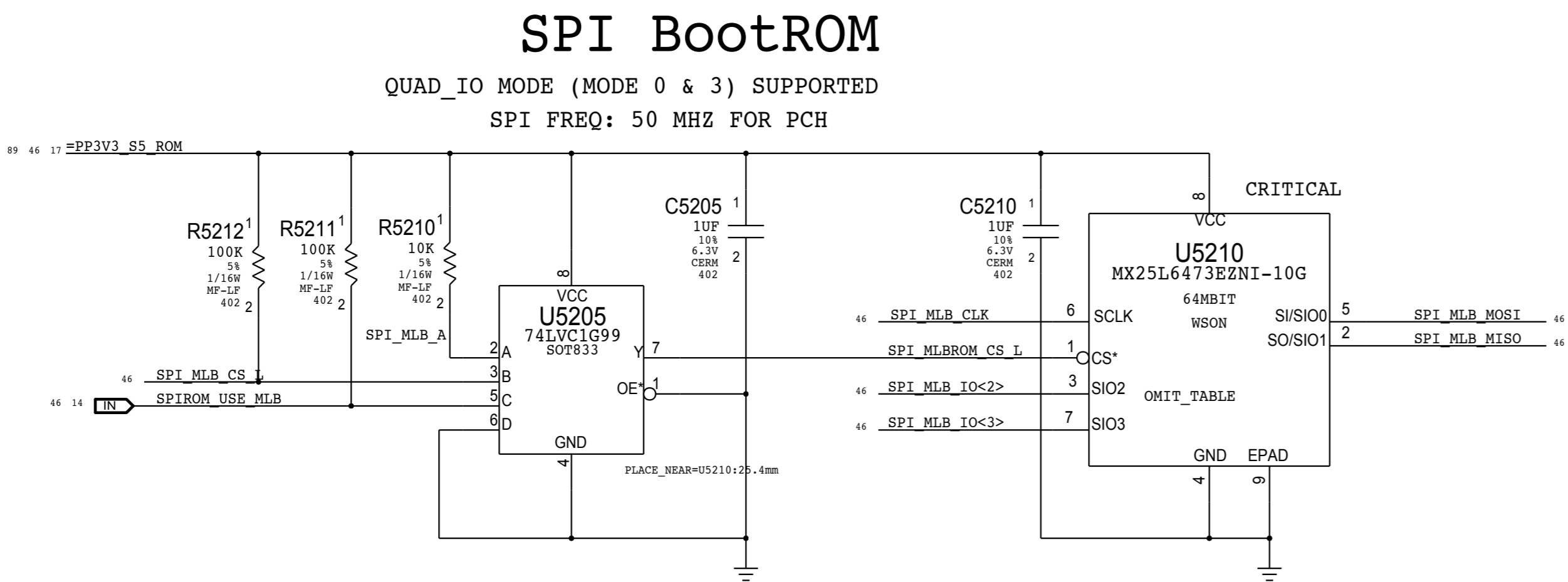
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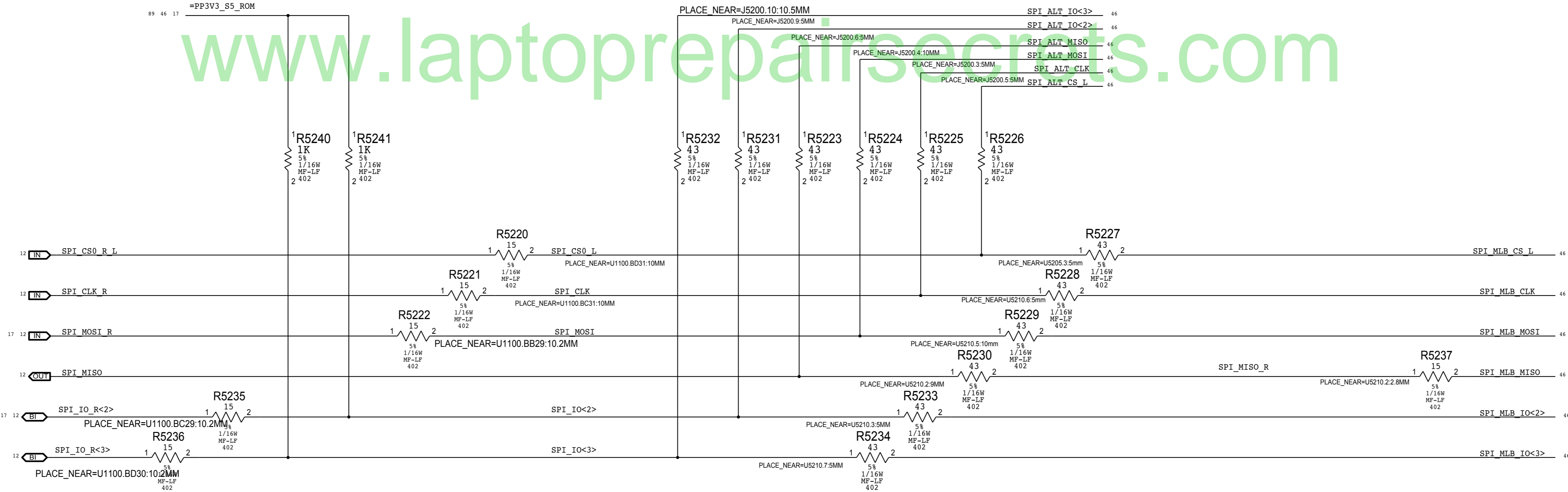
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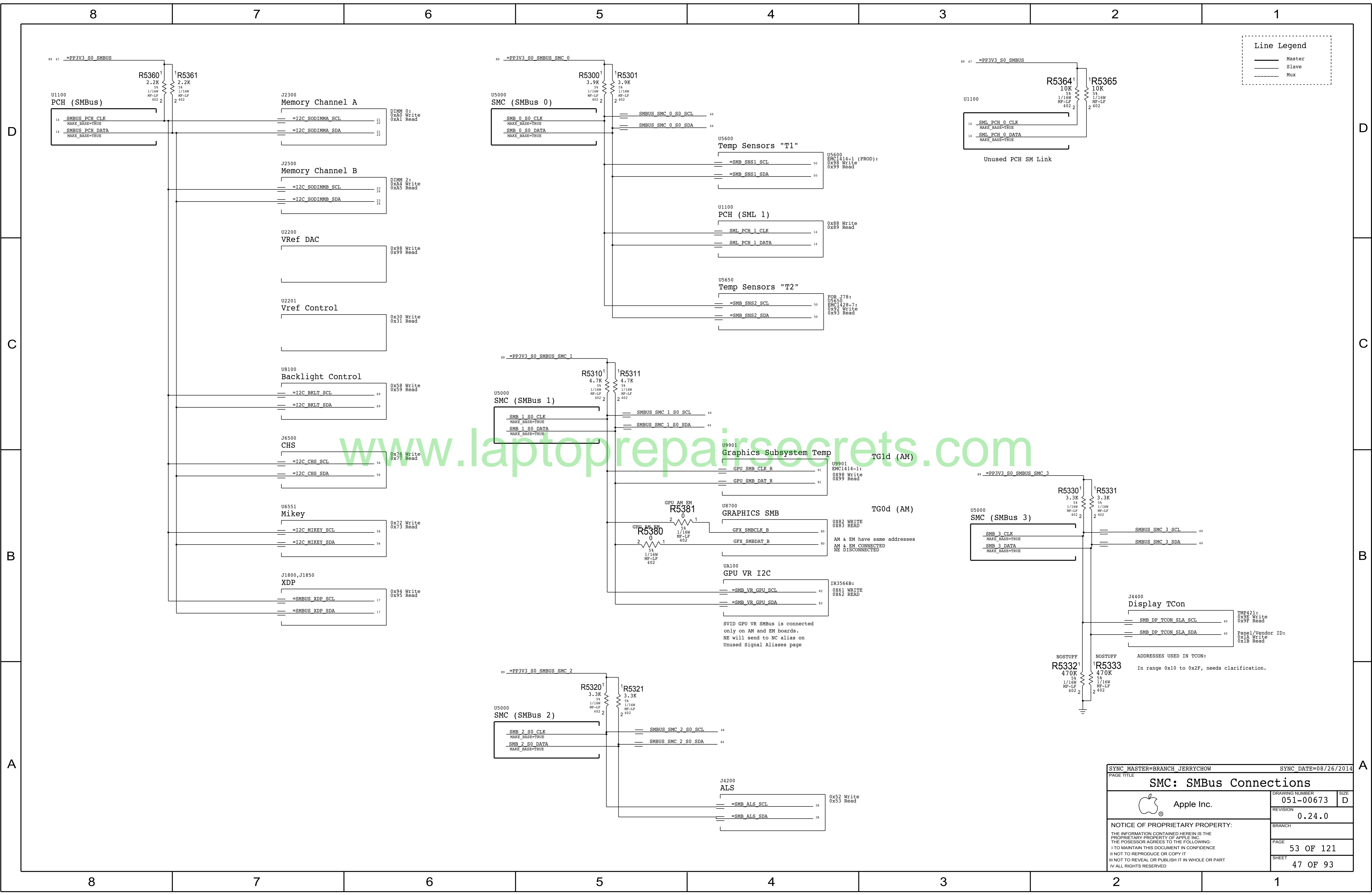
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SPI Series Termination



SYNC_MASTER=J17_TONY		SYNC_DATE=03/13/2013		
PAGE TITLE				
CPU & CHIPSET: SPI and Debug Connector				
	Apple Inc.	DRAWING NUMBER	051-00673	SIZE
		REVISION	0.24.0	
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		SHEET		46 OF 93



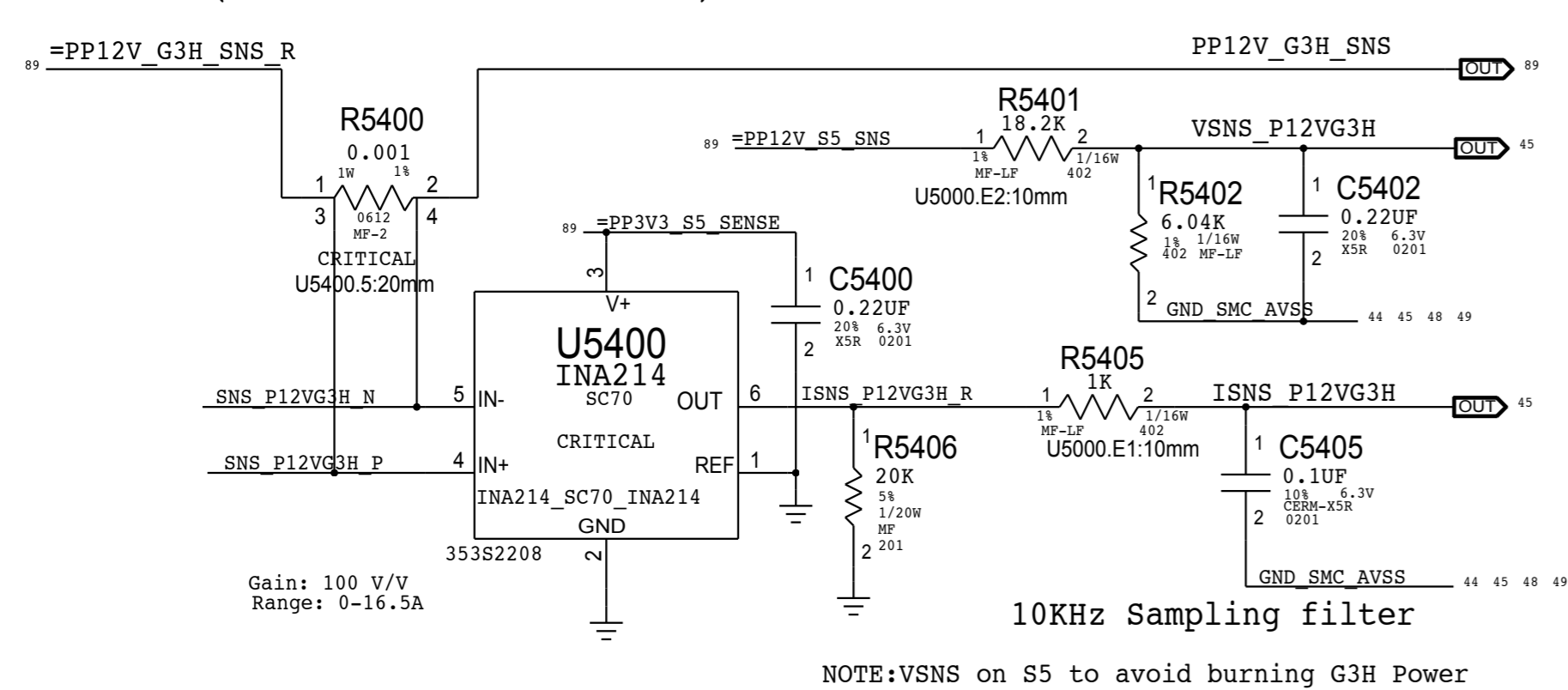
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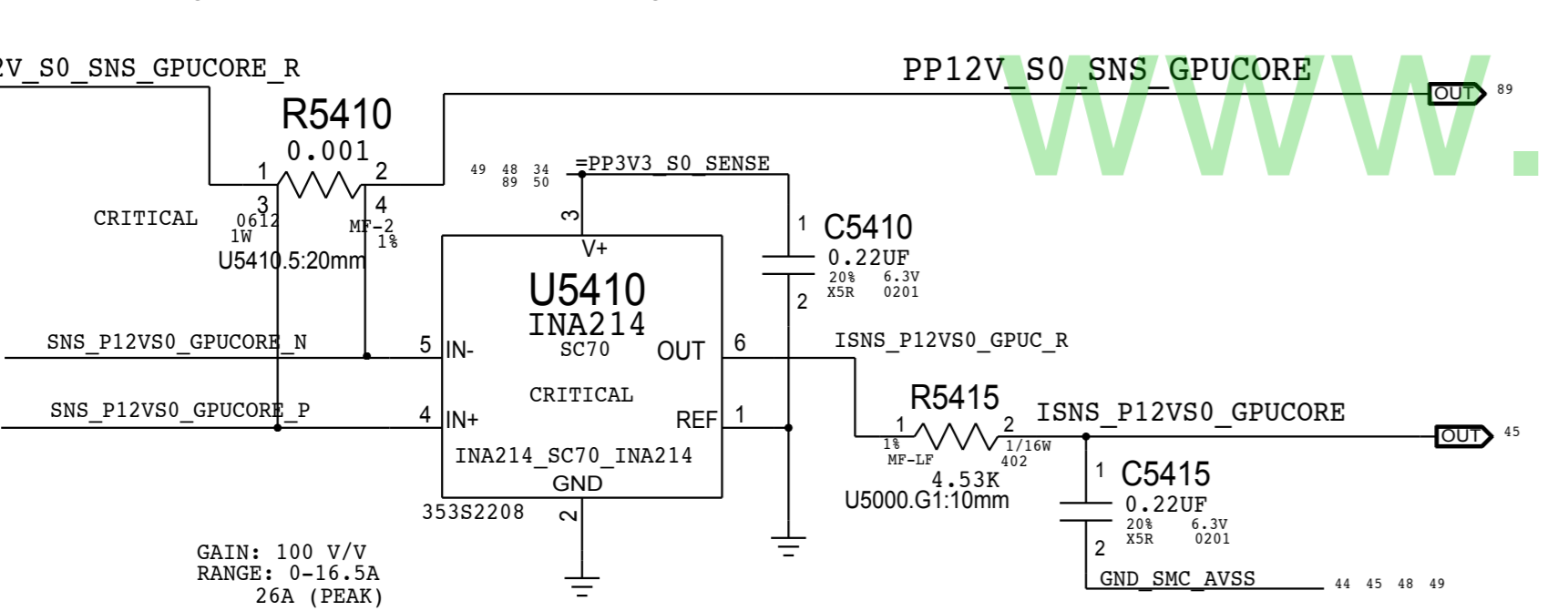
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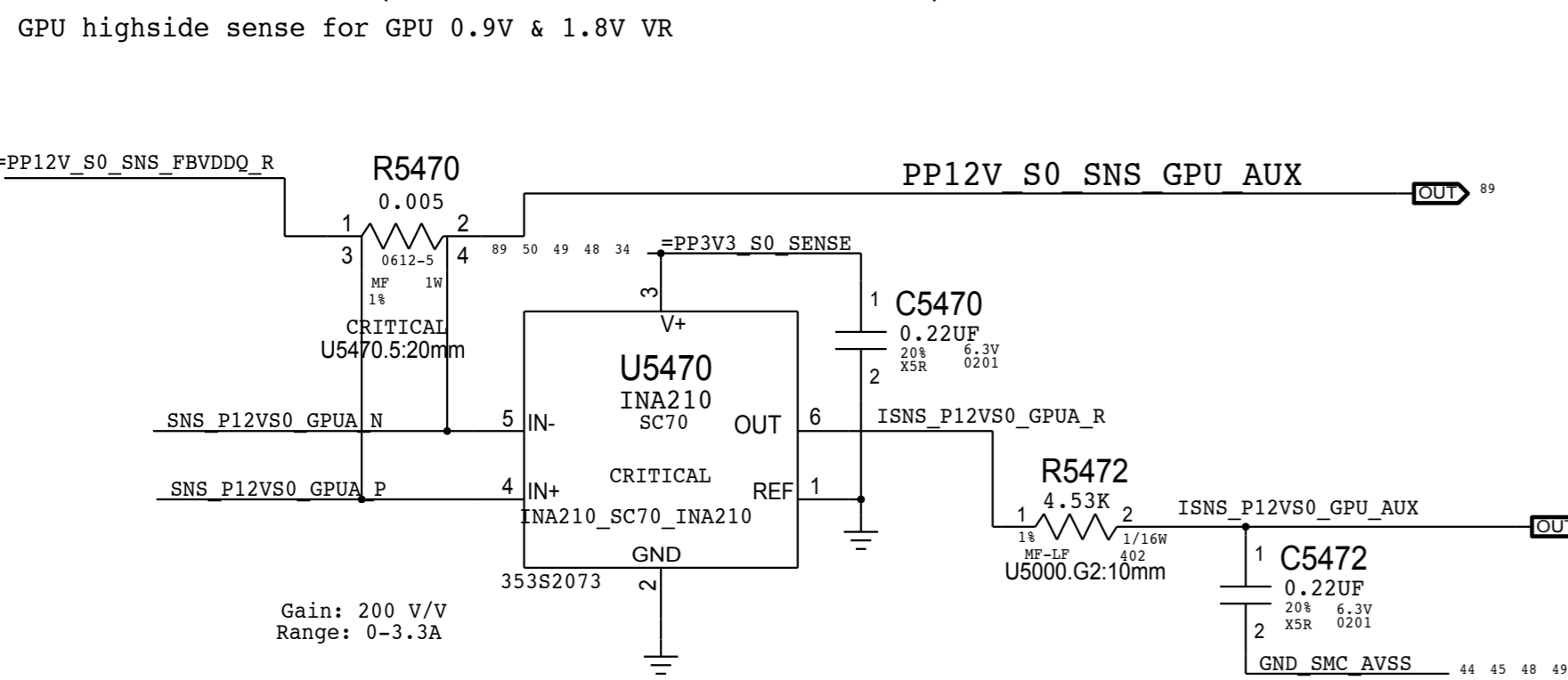
12V G3H (VD2R:ADC0/ID2R:ADC1)



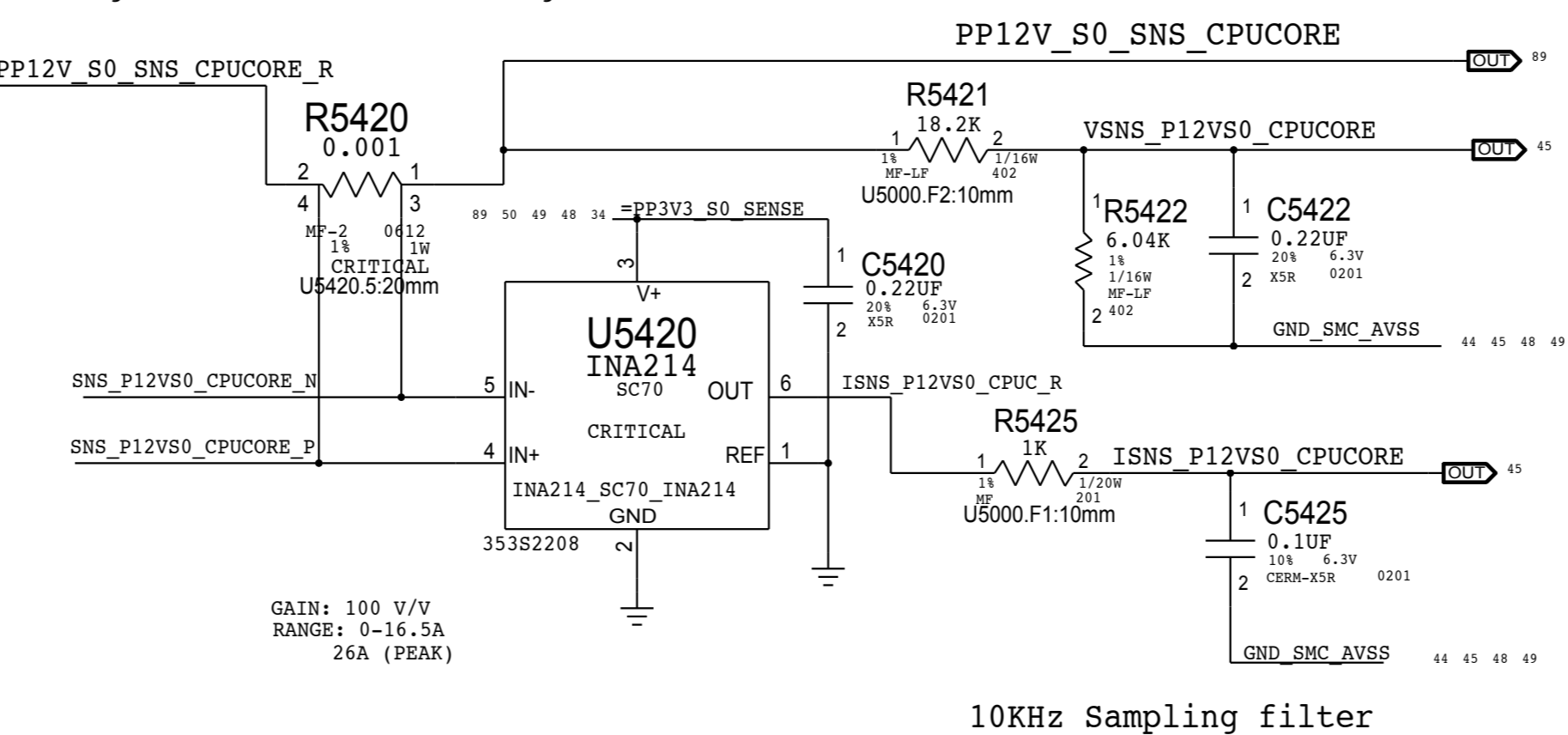
PP12V_S0_GPU (VG1C=VD20, IG1C:ADC17)



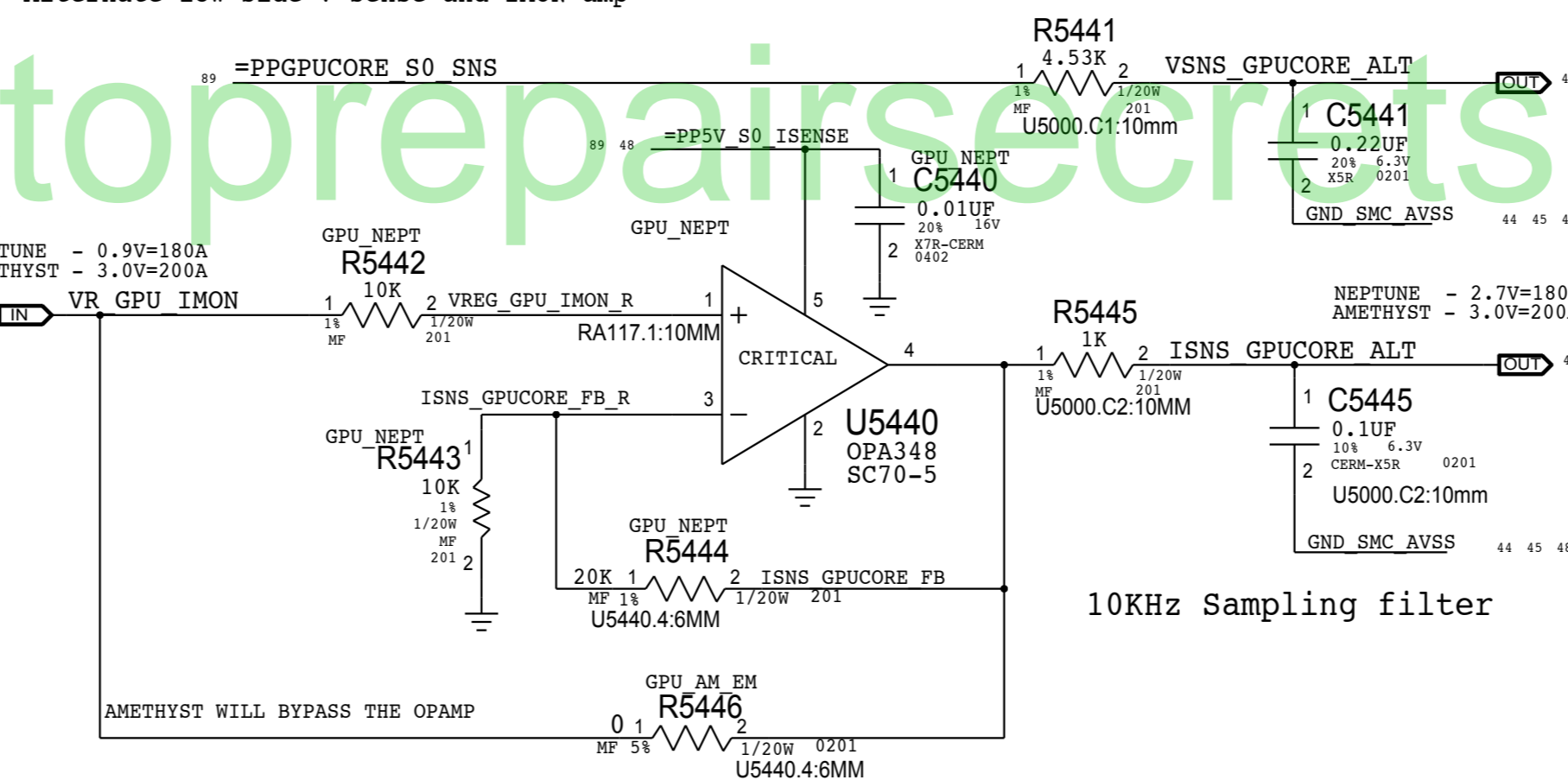
GPU AUX RAILS (VG1A=VD20, IG1A:ADC16)



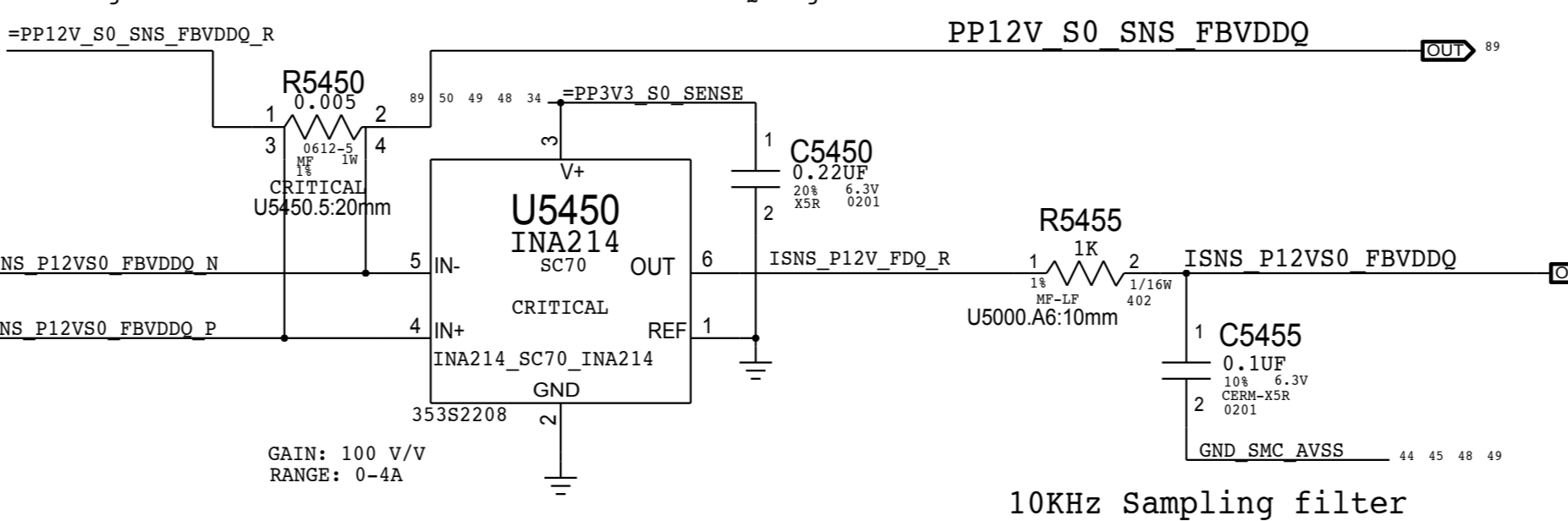
PP12V_S0_CPU (VD20:ADC2 /ID20:ADC3)



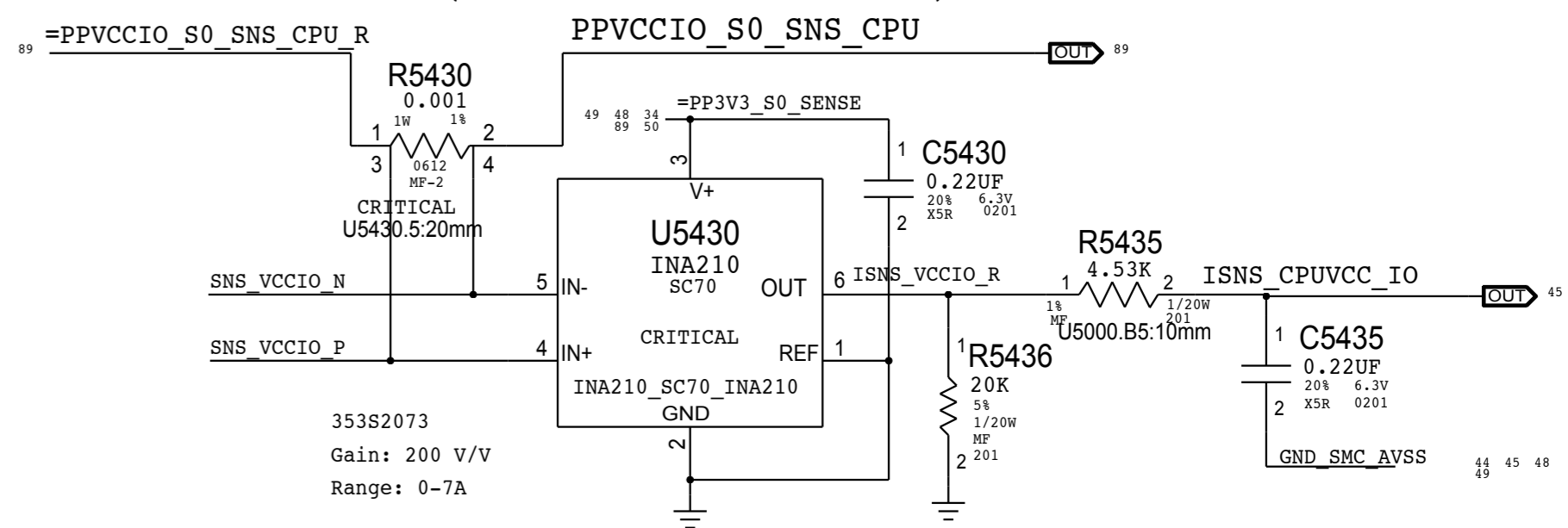
GPU Core - Alt (VG0C:ADC12/IG0C:ADC13)



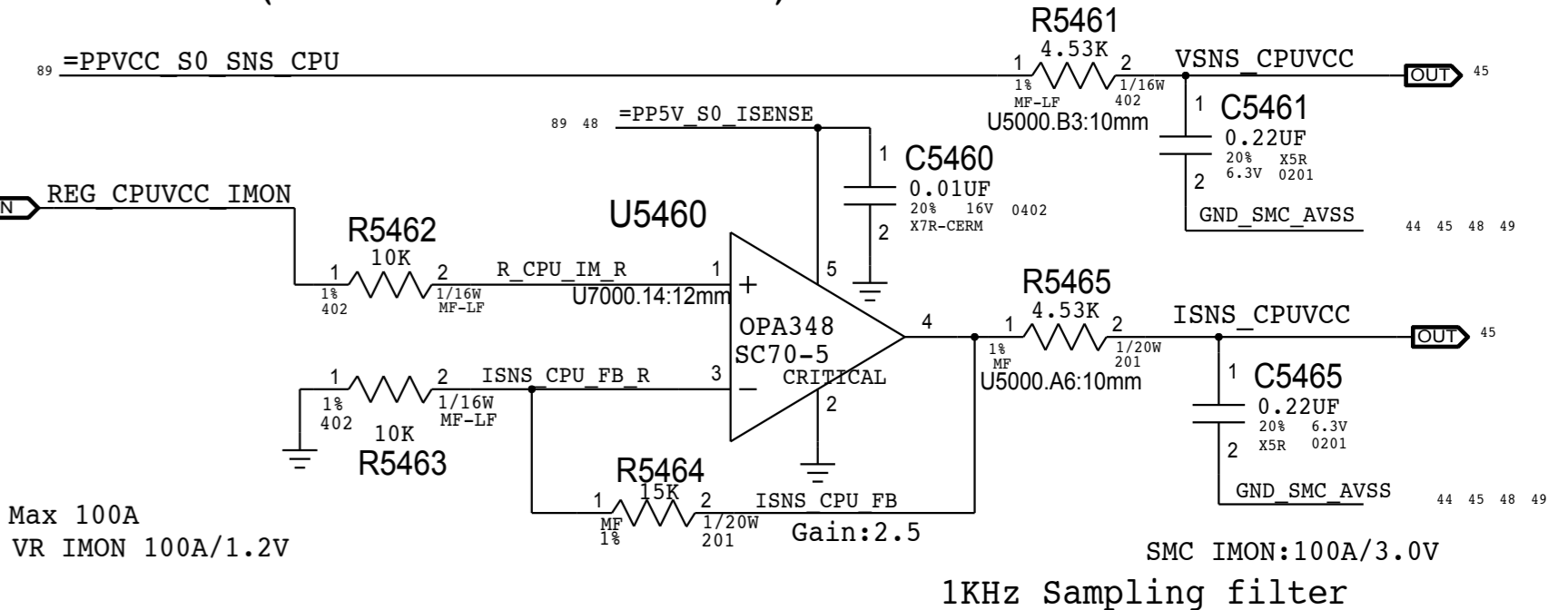
GPU FB (VG1F=VD20, IG1F:ADC11)



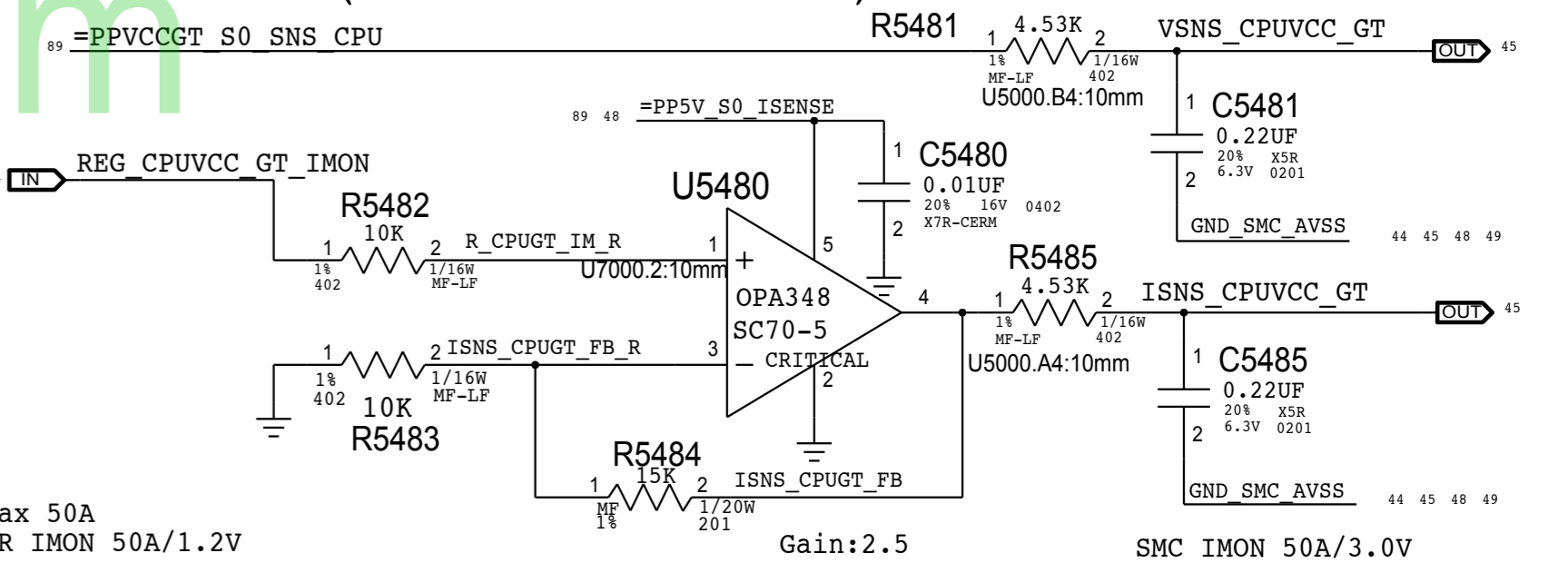
CPU VCCIO (VC0I=tbid, IC0I:ADC8)



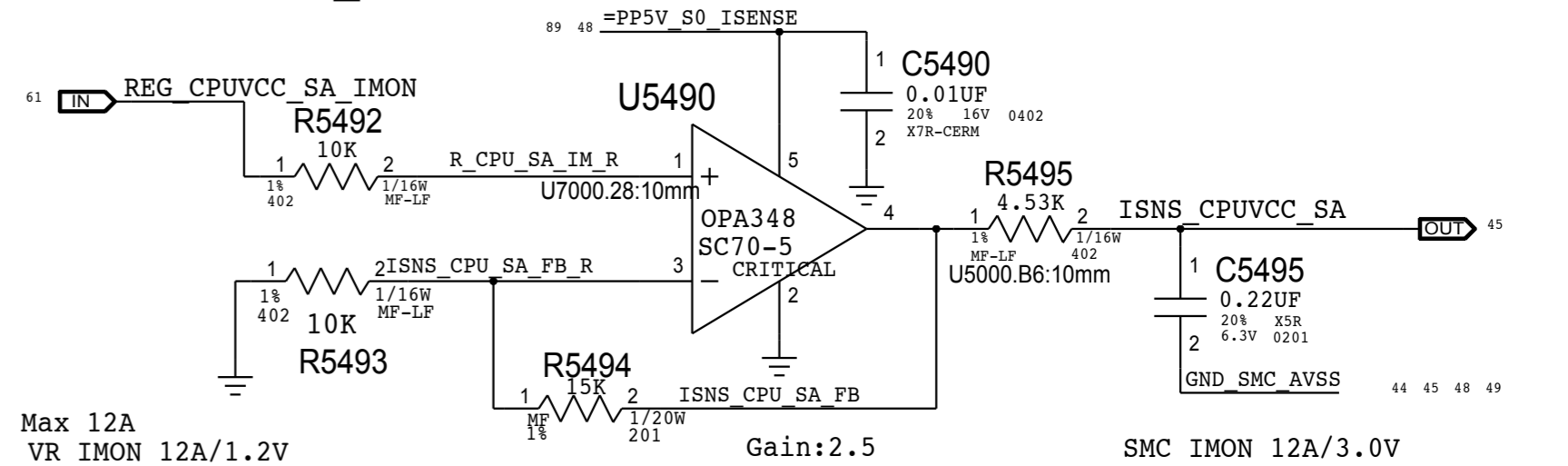
CPU Core (VC0C:ADC4/IC0C:ADC5)




CPU Core GT (VC0G:ADC6/IC0G:ADC7)



CPU Core VCC_SA (VC0S=1.05V, IC0S:ADC10)



SYNC_MASTER=BRANCH JERRYCHOW		SYNC_DATE=09/10/2014	
PAGE TITLE			
SENSORS: I and V Sense			
 Apple Inc.		DRAWING NUMBER	051-00673
		REVISION	0.24.0
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		PAGE	54 OF 121
		SHEET	48 OF 93

D

C

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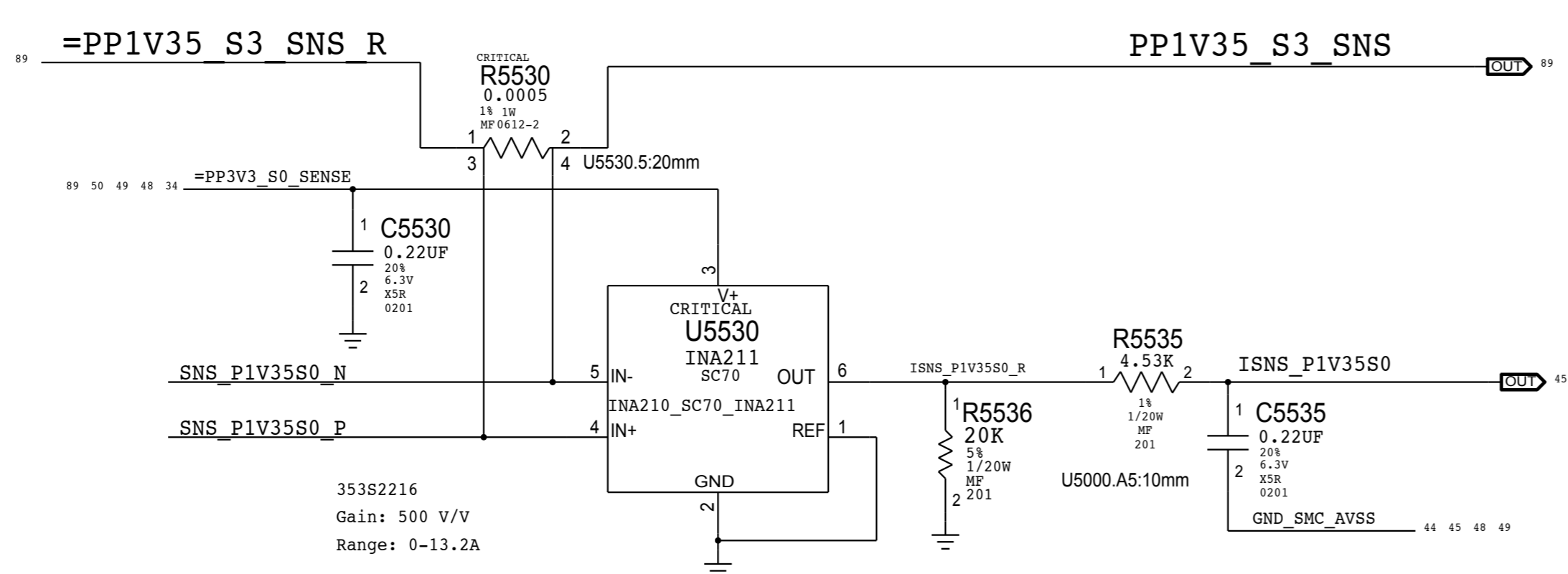
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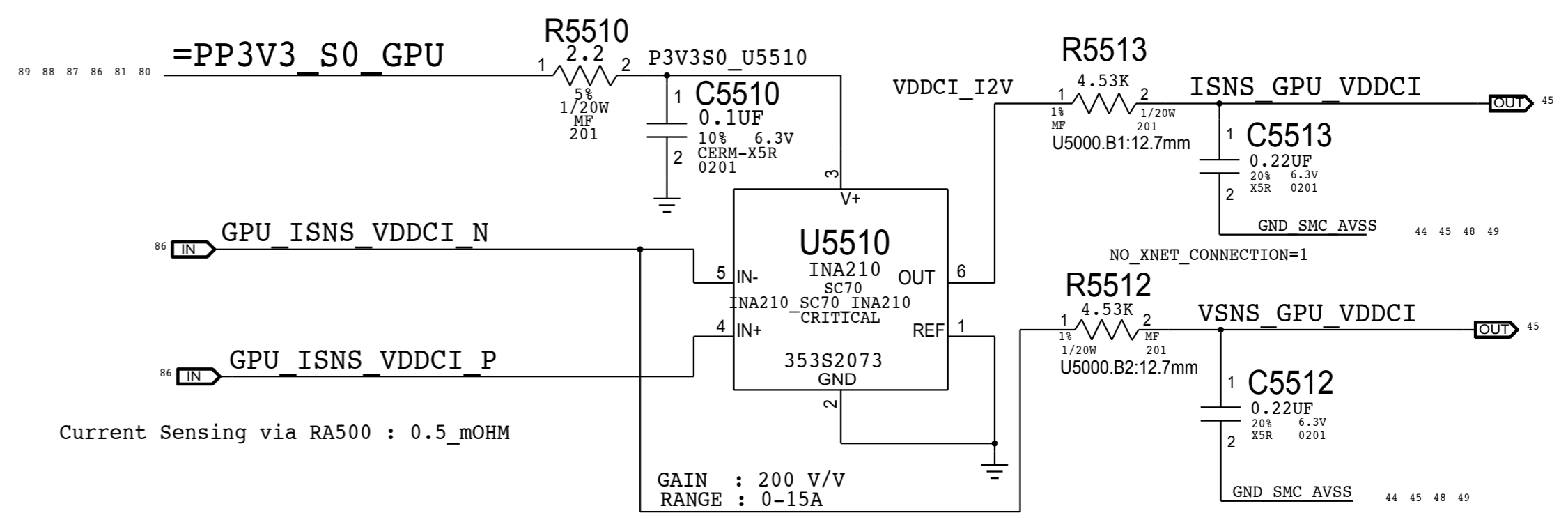
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VDDQ S3 (VCOM=VM0R, IC0M:ADC9)

VDDQ lowside sense for SO-DIMM modules

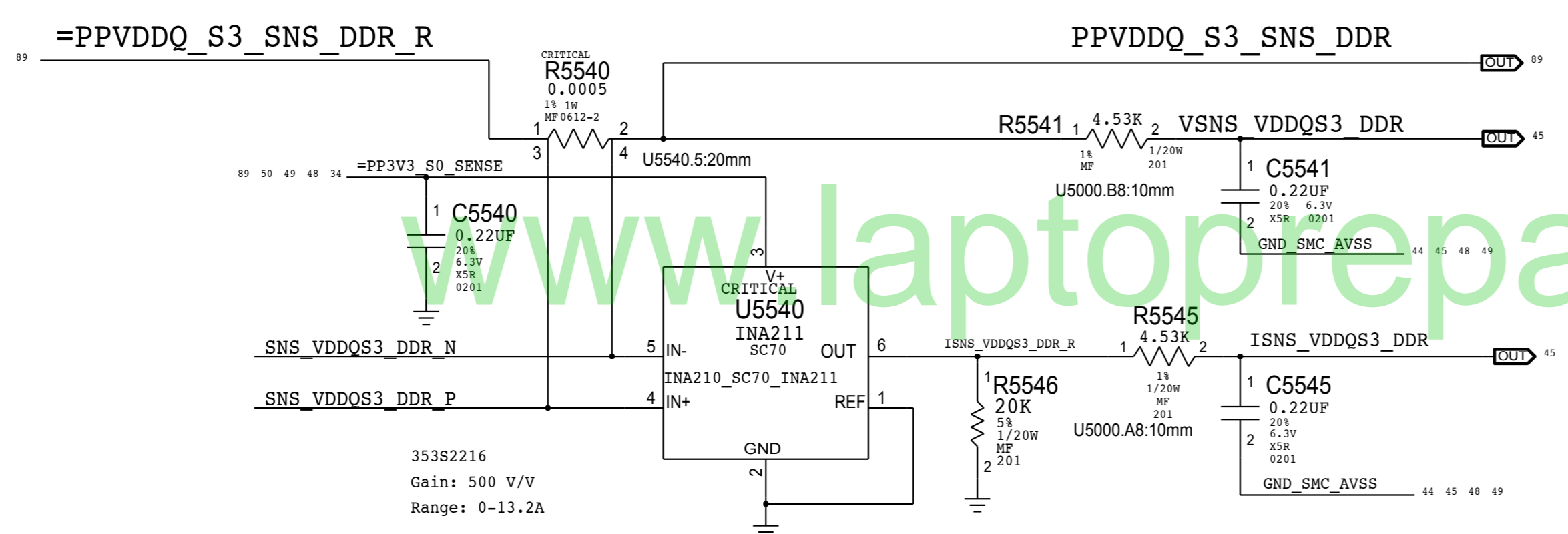


GPU_VDDCI S0 (VG0I:ADC14 /IG0I: ADC15)



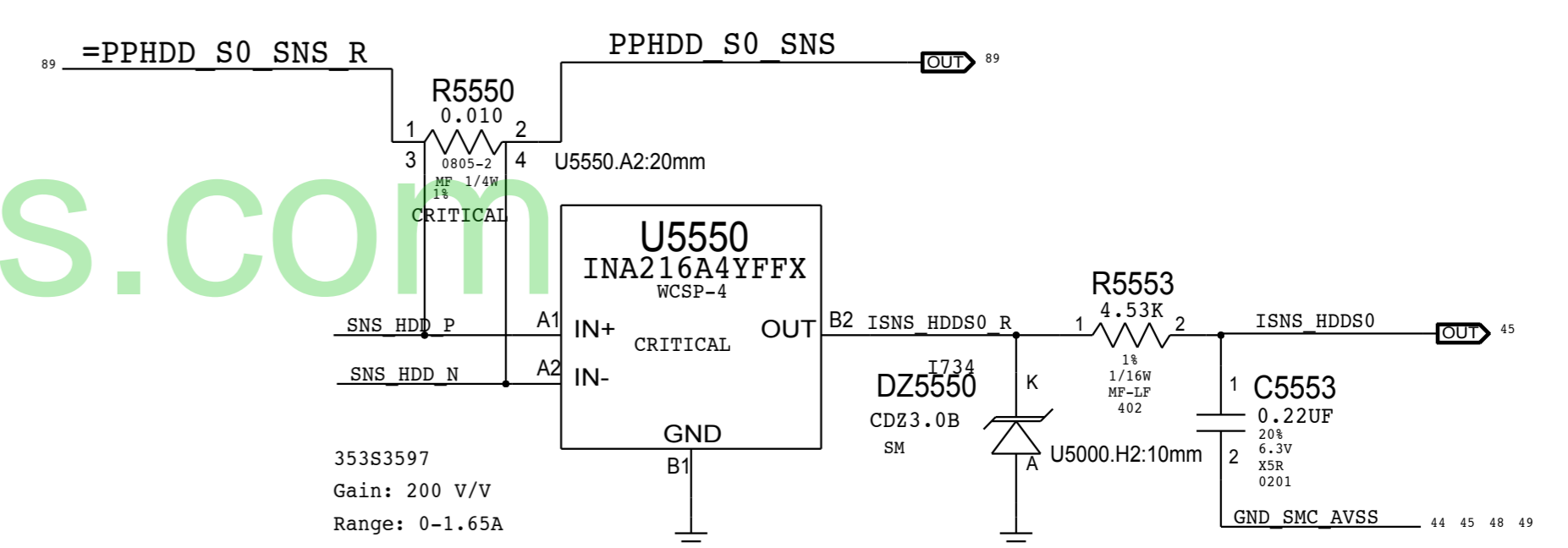
VDDQ S3 (VM0R:ADC22/ IM0R:ADC23)

VDDQ lowside sense for SO-DIMM modules



HDD S0 (VH05=5V, IH05:ADC19)

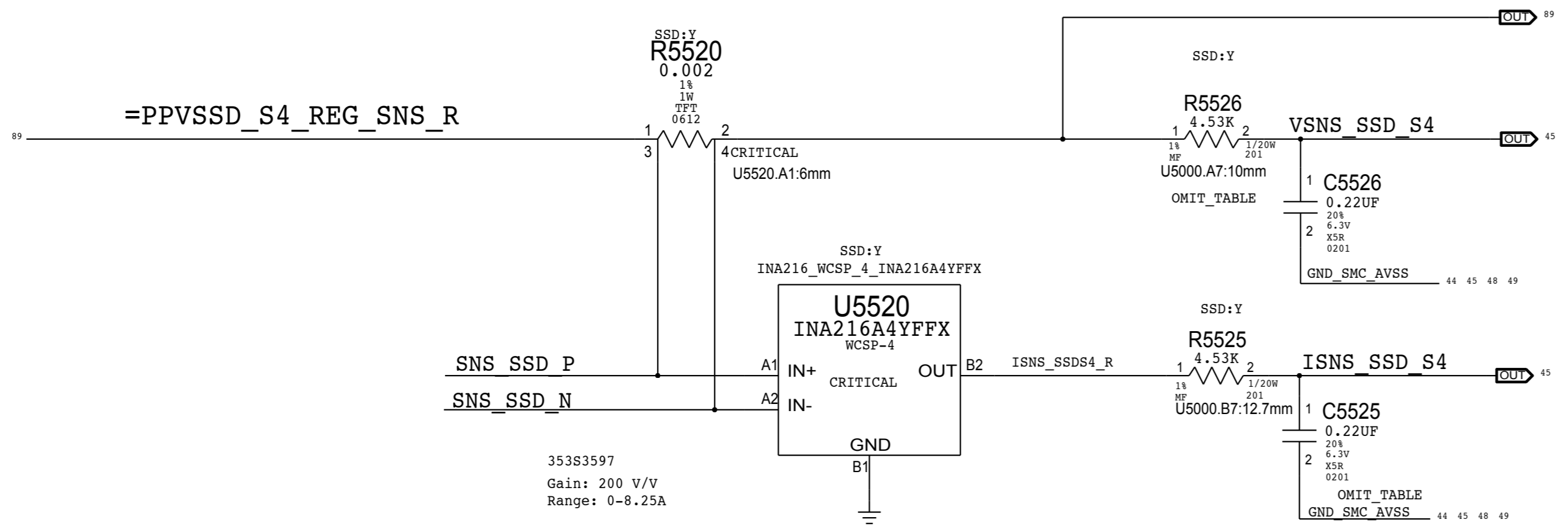
I/V-sense for HDD 5V



SSD S4 (VR1R:ADC20 / IH1R:ADC21)

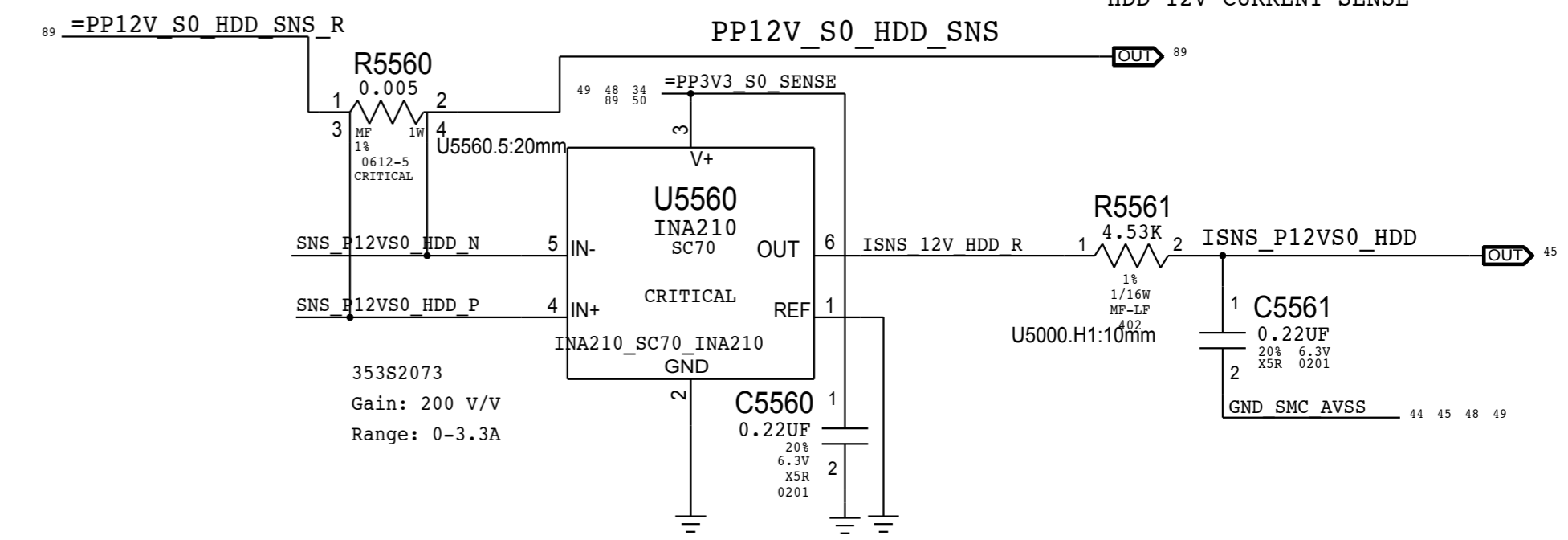
I-SENSE FOR SSD / V-SENSE FOR PPSSD_S4)

PPVSSD_S4_REG SNS



PP12V_S0_HDD (VH02=VD20, IH02:ADC18)

HDD 12V CURRENT SENSE



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
13280304	2	CAP, 0.22UF, 201	C5525,C5526	SSD:Y
11780201	2	RES, 0 OHM, 201	C5525,C5526	SSD:N

SYNC_MASTER=BRANCH_JERRYCHOW

SYNC_DATE=09/10/2014

DRAWING NUMBER

051-00673

SIZE

D

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PAGE

55 OF 121

SHEET

49 OF 93

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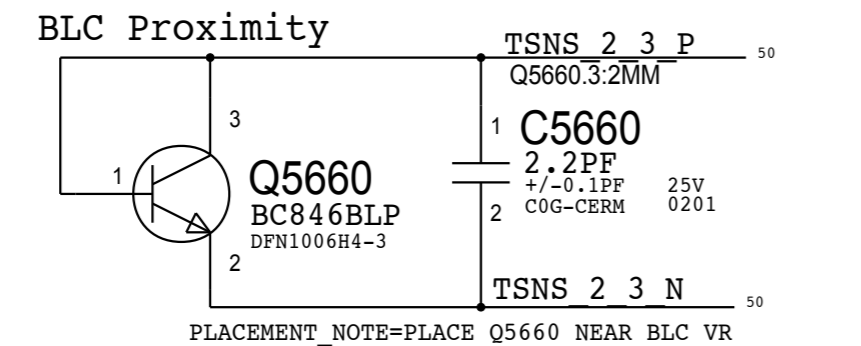
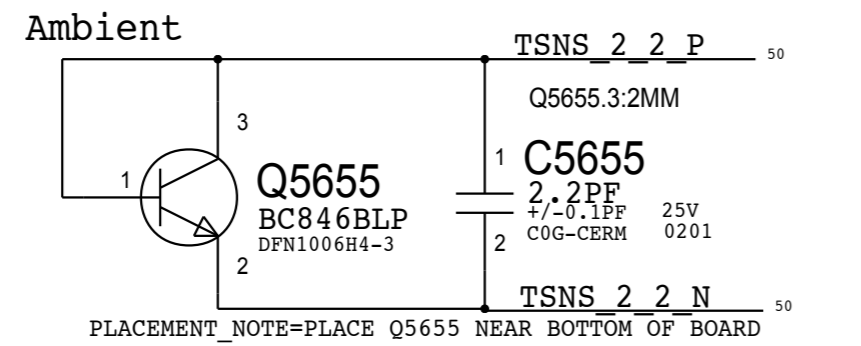
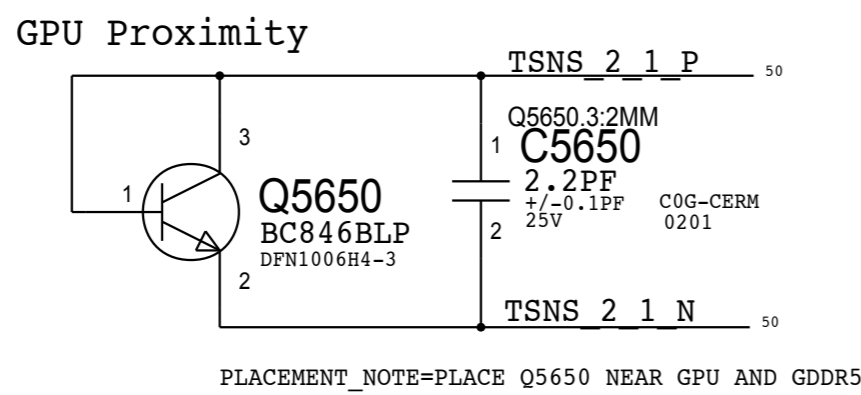
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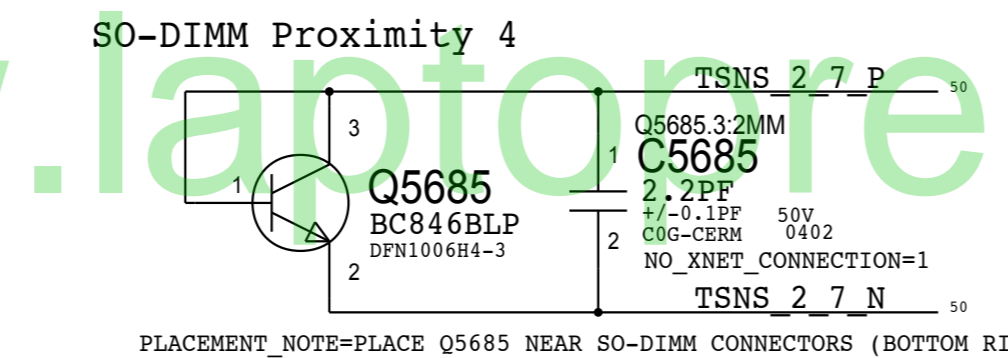
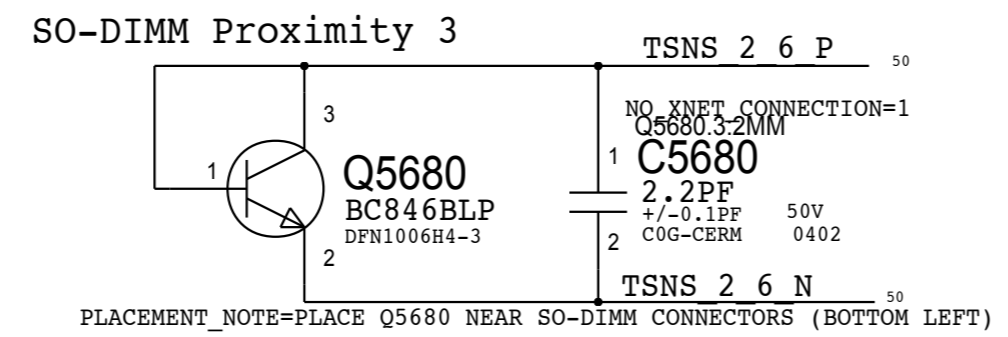
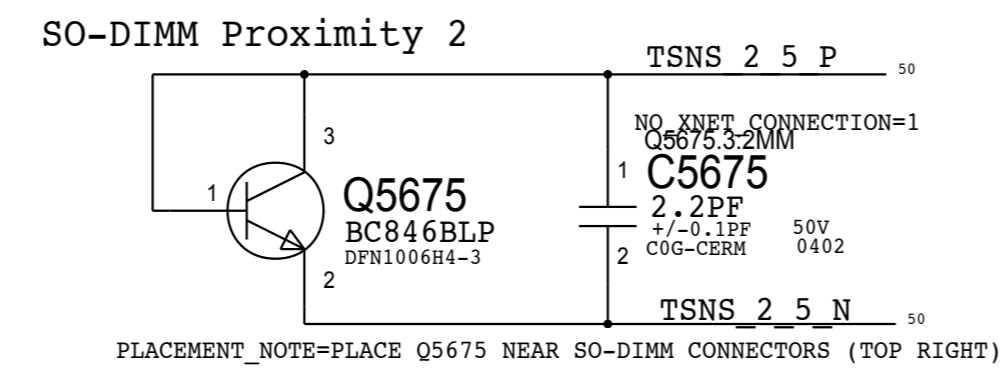
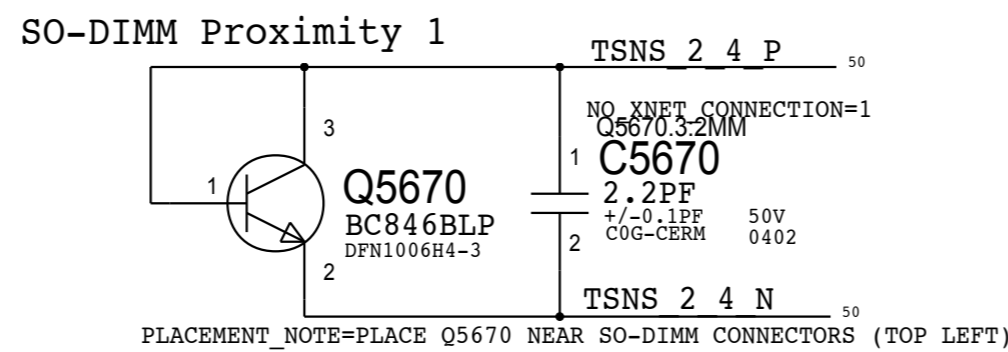
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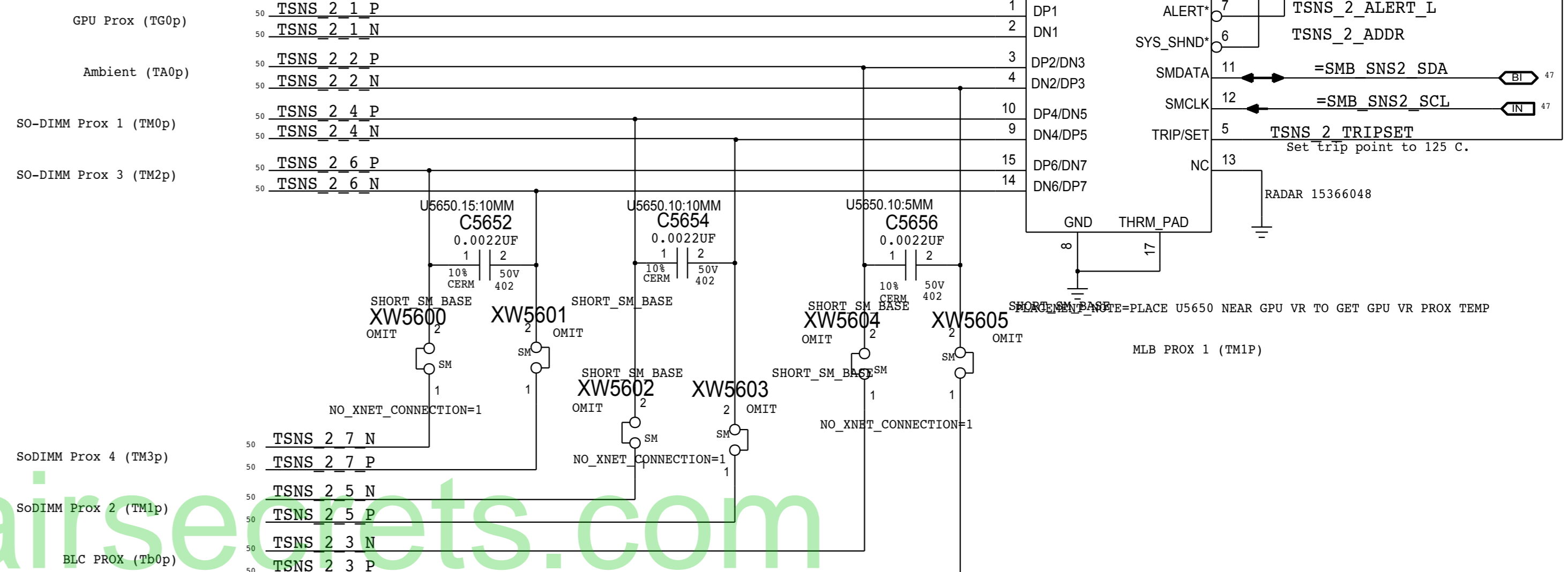


NEED TO FIND LOCATION

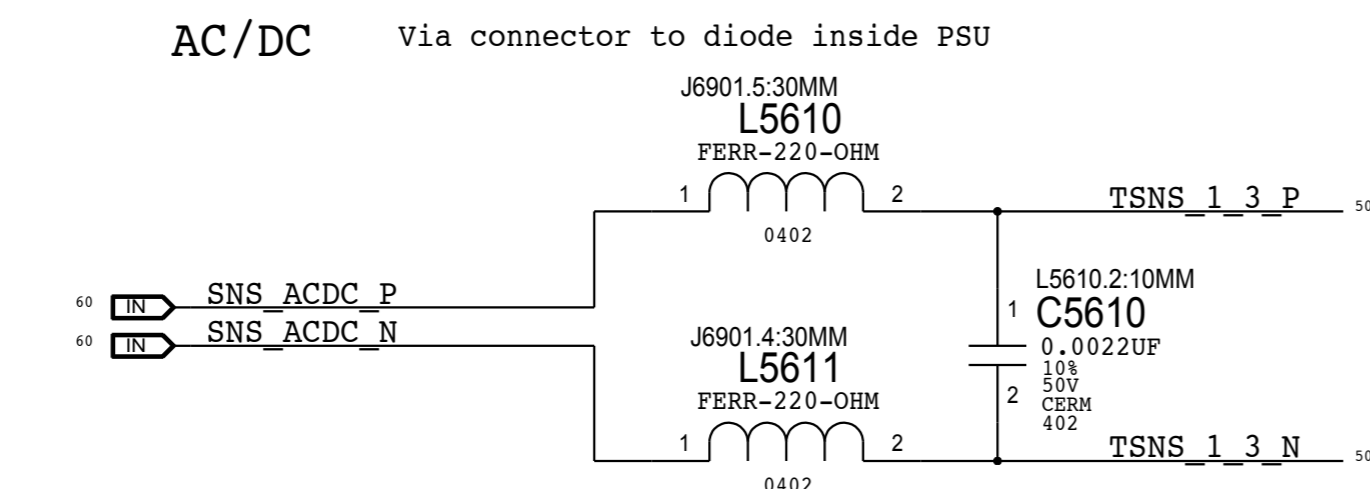
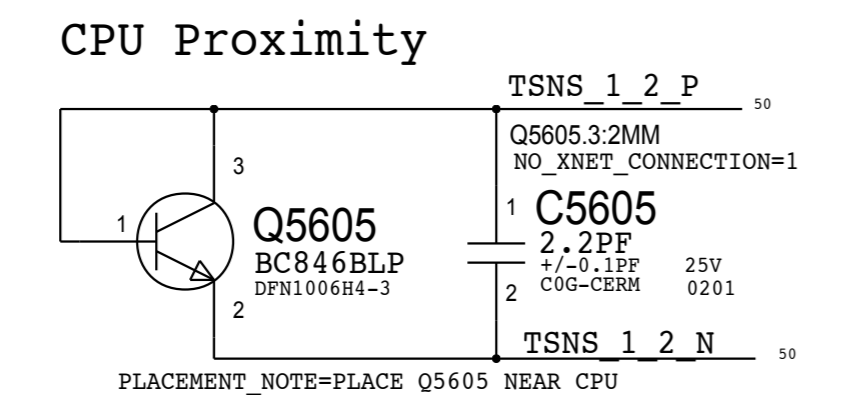
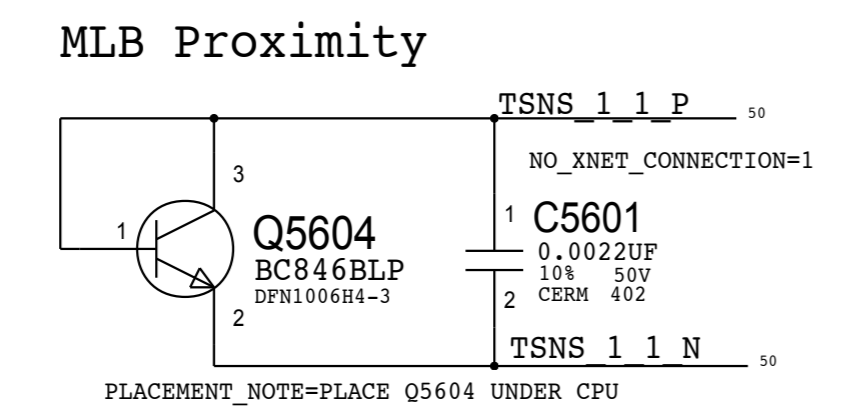


TEMP SENSOR T2 EMC1428: NEAR GPU VR

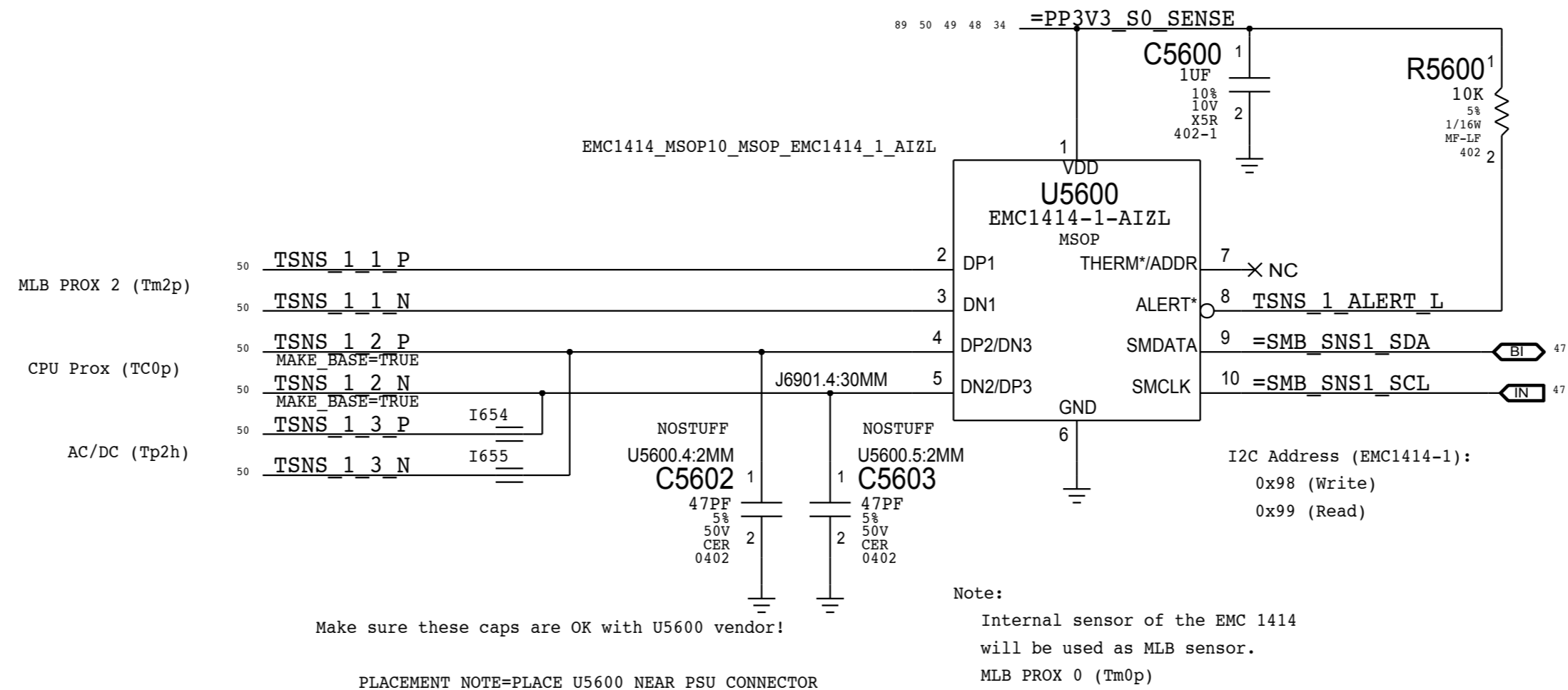
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
37280186	37280185		ALL	Alternate Temp Diode



EMC1428-7: 6.8K PULL UP: I2C ADDRESS: WRITE: 0x92, READ: 0x93



Temperature Sensor T1 EMC1414: Near PSU Conn

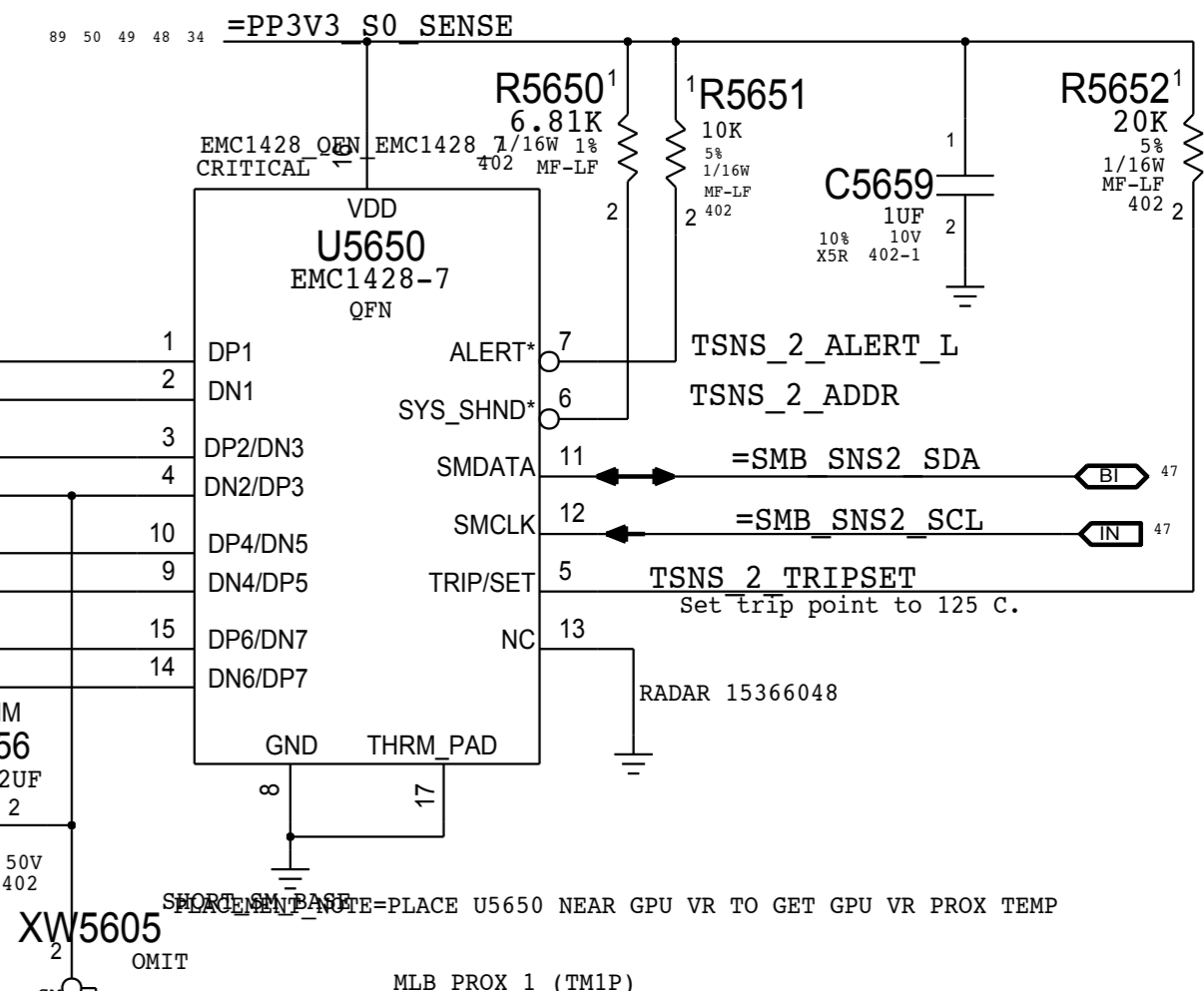



Make sure these caps are OK with U5600 vendor!

PLACEMENT_NOTE=PLACE U5600 NEAR PSU CONNECTOR

Note:
Internal sensor of the EMC 1414
will be used as MLB sensor.
MLB PROX 0 (Tm0p)

SNS T2: TEMP SENSOR IC



SYNC MASTER=BRANCH JERRYCHOW		SYNC DATE=09/10/2014	
PAGE TITLE			
SENSORS: Temperature Sensors			
 Apple Inc.		DRAWING NUMBER	051-00673
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		PAGE	56 OF 121
		SHEET	50 OF 93

D

C

B

A

D

C

B

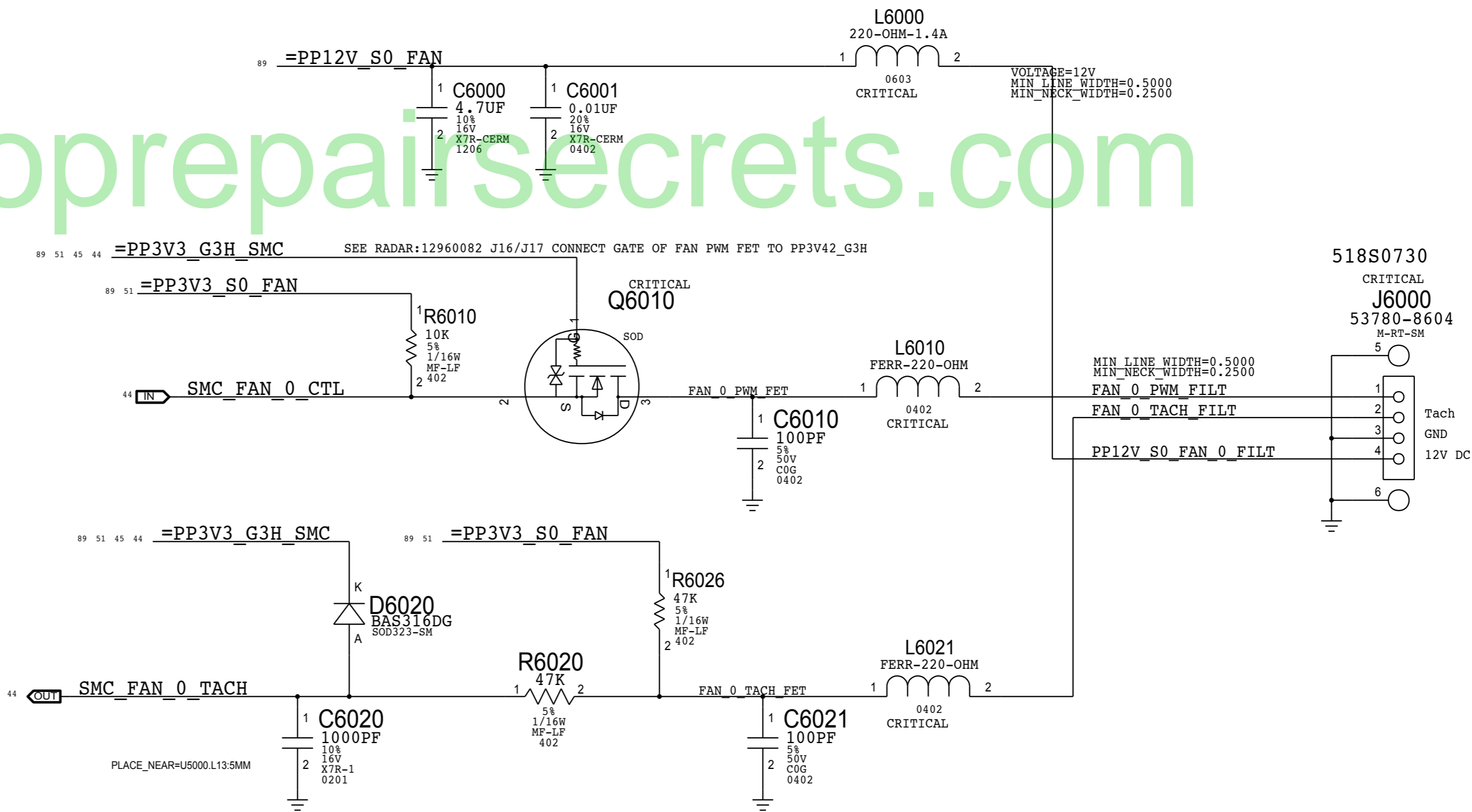
A

SMC Fan 0 (System)

Note:
The circuit for the PWM input to the fan acts as a non-inverting level-shifter to protect the SMC. It is assumed there is a pull-up to 5V/12V inside the fan, otherwise when the SMC PWM goes low and Q6010 turns on, there would be 5V/12V present on the SMC pin! Then by definition, the drain of Q6010 is at common and the SMC sinks current when Q6010 is on.

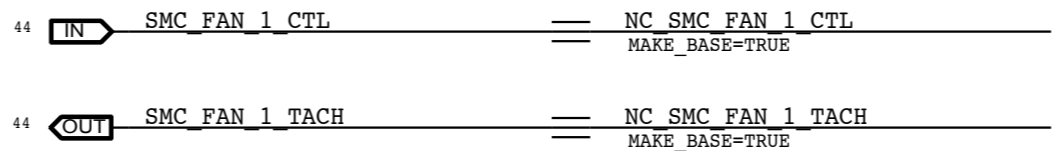
This resembles an open-drain if there is a pull-up, going to a Hi-Z FET input.


Otherwise, this is simply a pass-FET.
See RADAR: 10565825- D7: Need scematic and PCB file of fan(All Vendors).

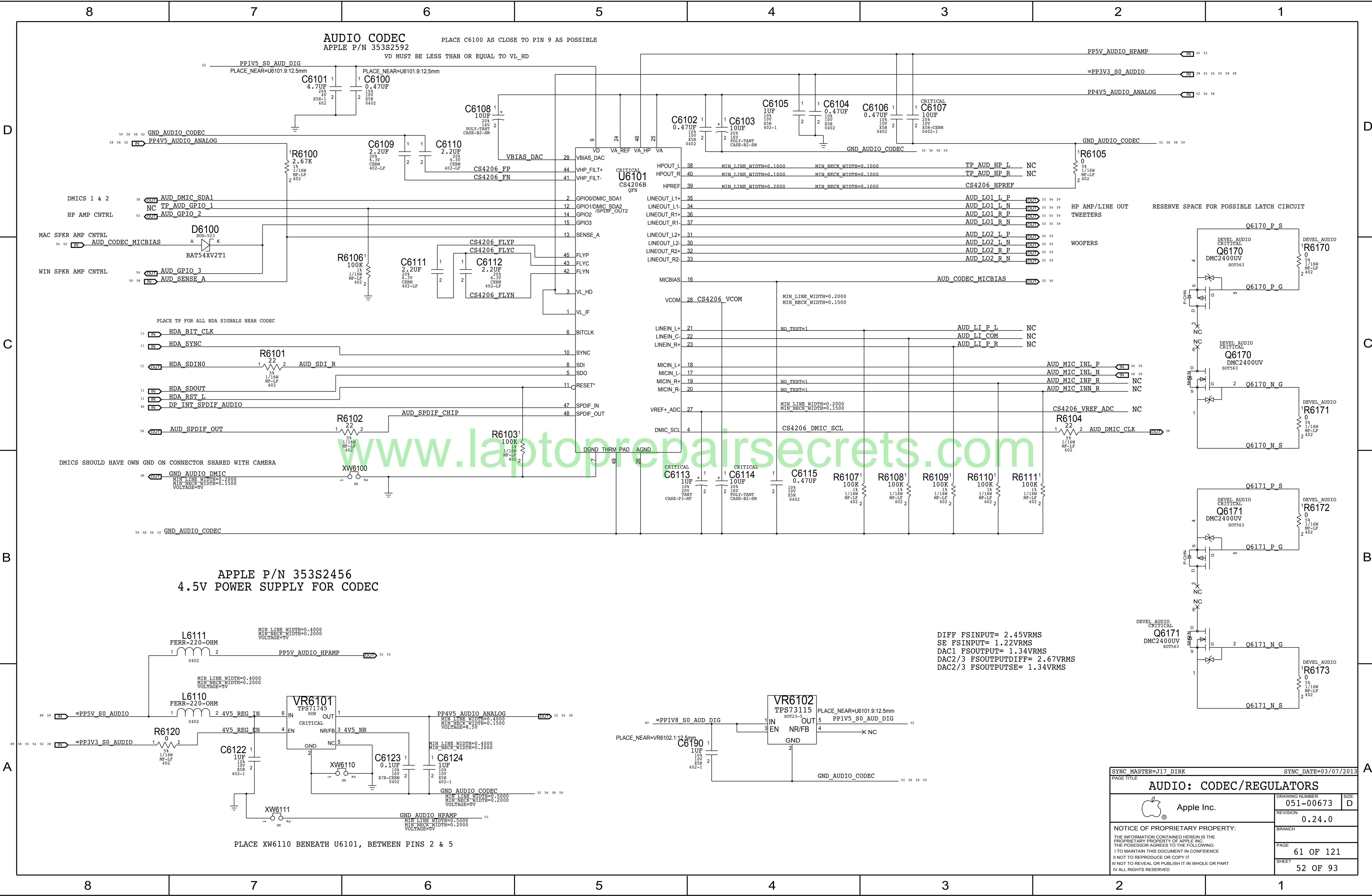


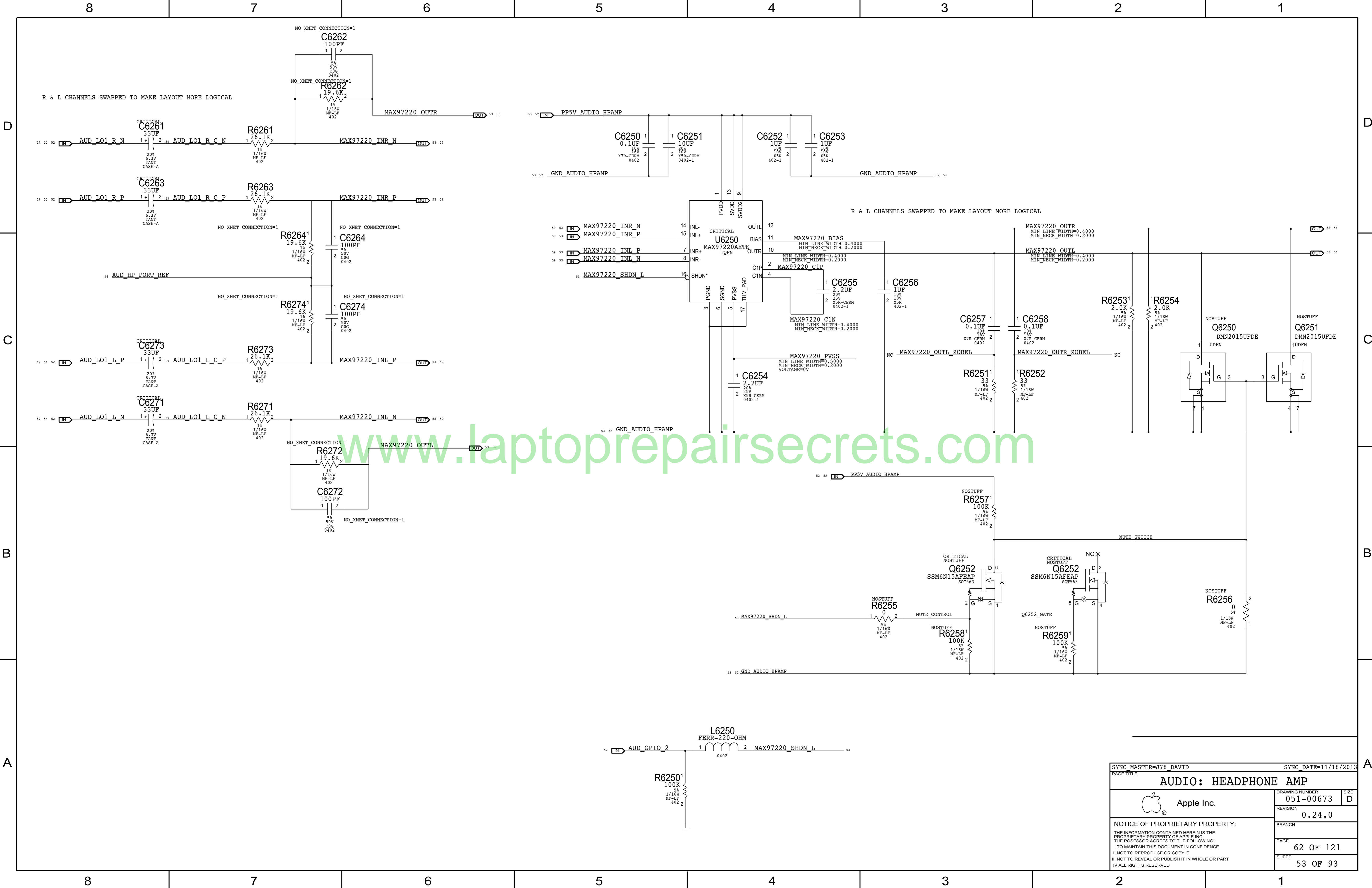
Add C6020 1000pF Cap, Change R6020 to 47K -- Radar 11661918 D8 Protol Fan Tach instability.

SMC Fan 1 (Unused)



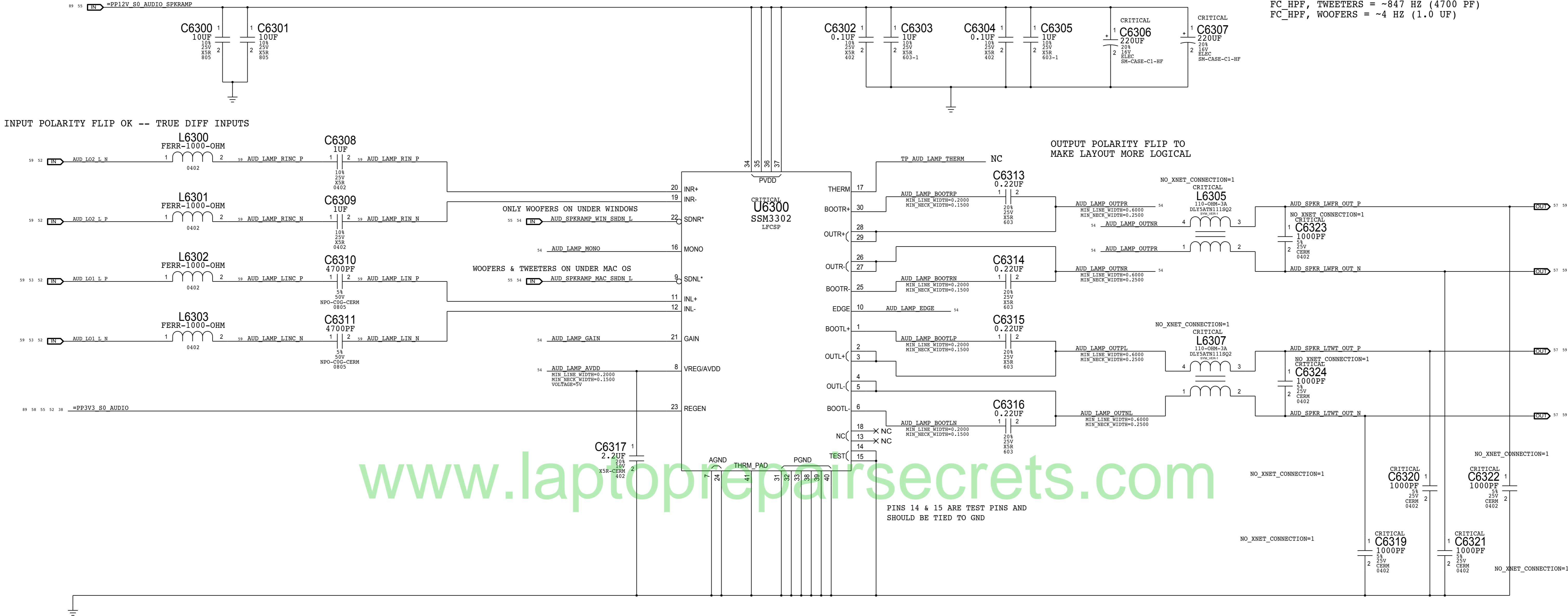
SYNC_MASTER=J16_IG		SYNC_DATE=04/29/2013	
PAGE TITLE			
FAN: System Fan			
	Apple Inc.	DRAWING NUMBER	051-00673
		SIZE	D
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		BRANCH	
		PAGE	60 OF 121
		SHEET	51 OF 93





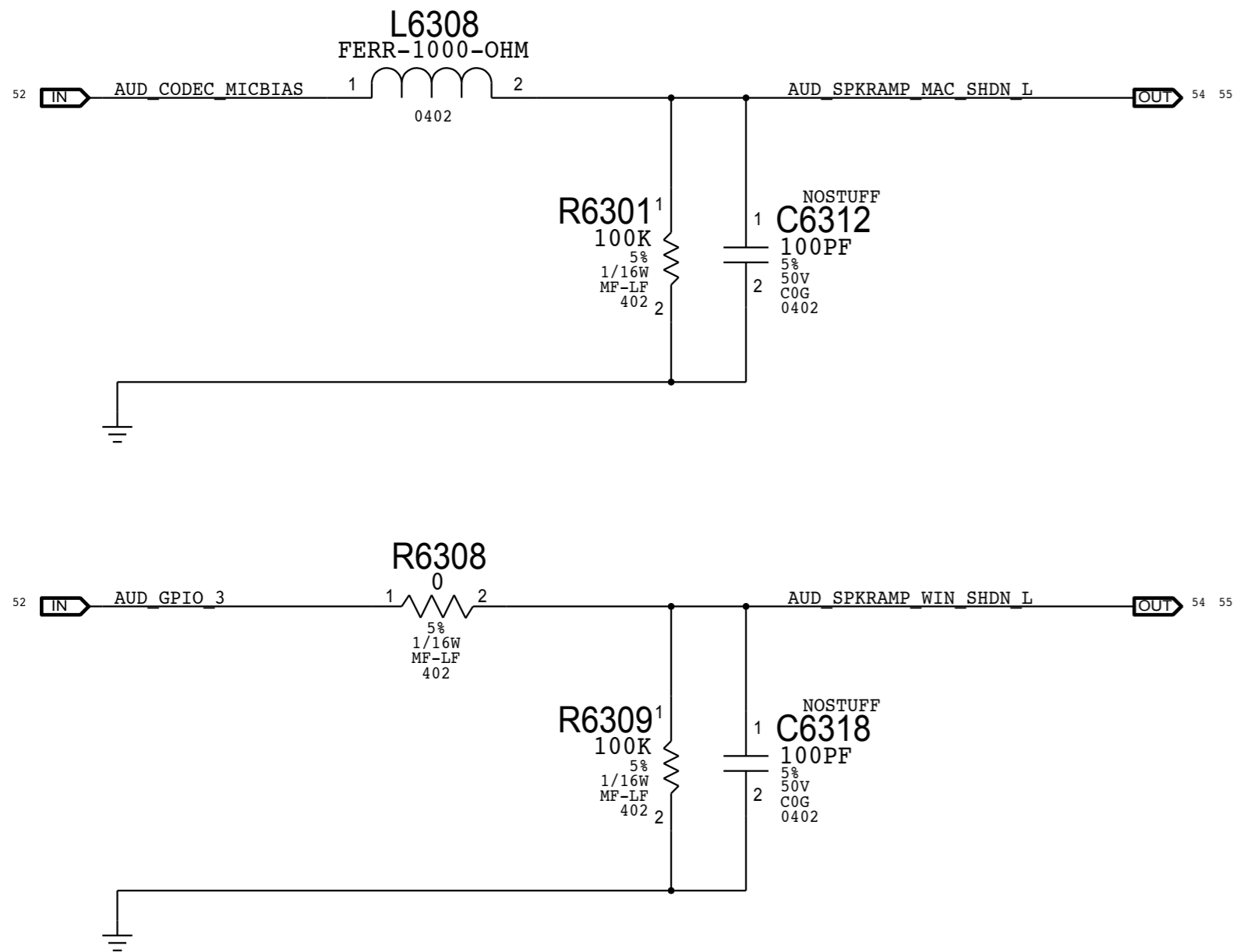
LEFT CH SPEAKER AMP
APPLE P/N 353S3163

SPEAKER AMP GAIN = +12 DB
SPEAKER AMP RIN = 40K NOMINAL
FC_HPF, TWEETERS = ~847 HZ (4700 PF)
FC_HPF, WOOFERS = ~4 HZ (1.0 UF)



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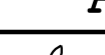
PINS 14 & 15 ARE TEST PINS AND
SHOULD BE TIED TO GND



EDGE RATE
CONTROL R6304 R6305
ON 0 OHM NOSTUFF
OFF NOSTUFF 0 OHM

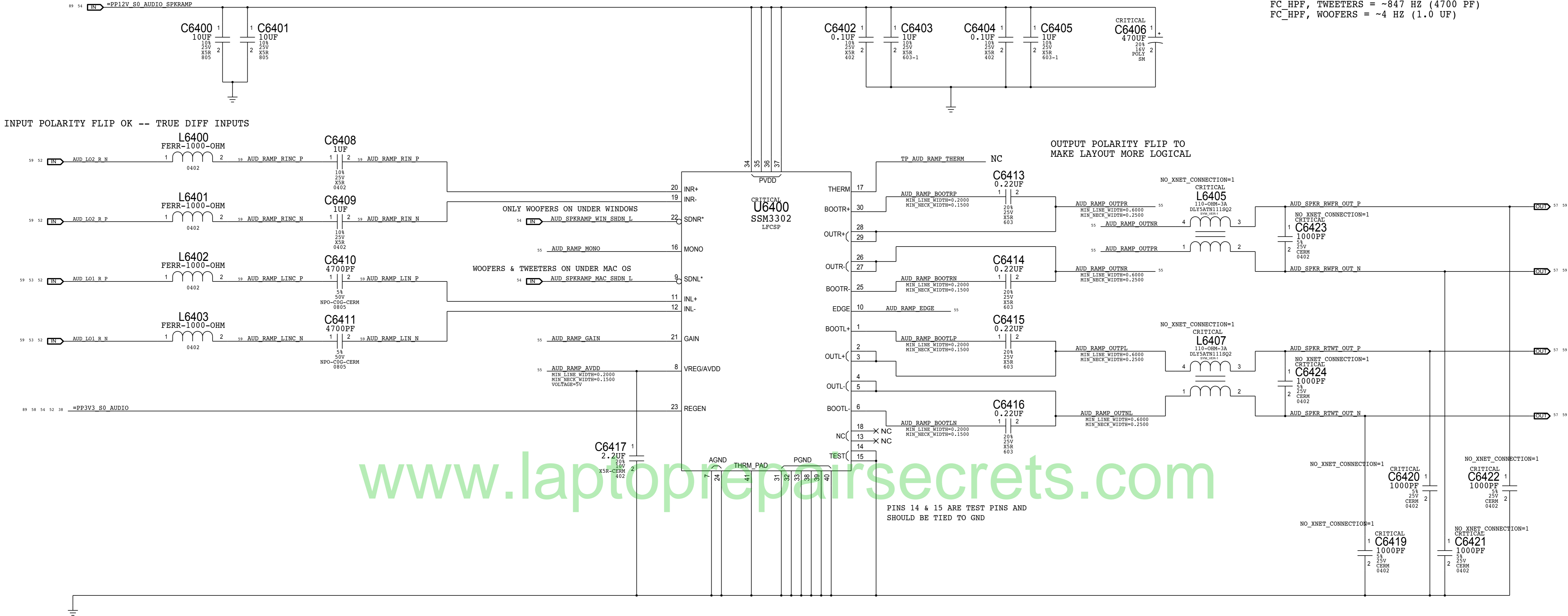
AUD RAMP MONO NET:
HIGH = MONO OPERATION
LOW = STEREO OPERATION

GAIN R6306 R6307
+9 DB NOSTUFF 0 OHM
+12 DB NOSTUFF 47 KOHM
+15 DB NOSTUFF NOSTUFF
+18 DB 47 KOHM NOSTUFF
+24 DB 0 OHM NOSTUFF

SYNC MASTER=J78 DAVID		SYNC DATE=11/18/2013	
PAGE TITLE			
AUDIO: LEFT SPKR AMP			
 Apple Inc.		DRAWING NUMBER	051-00673
		REVISION	0.24.0
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		PAGE	63 OF 121
		SHEET	54 OF 93

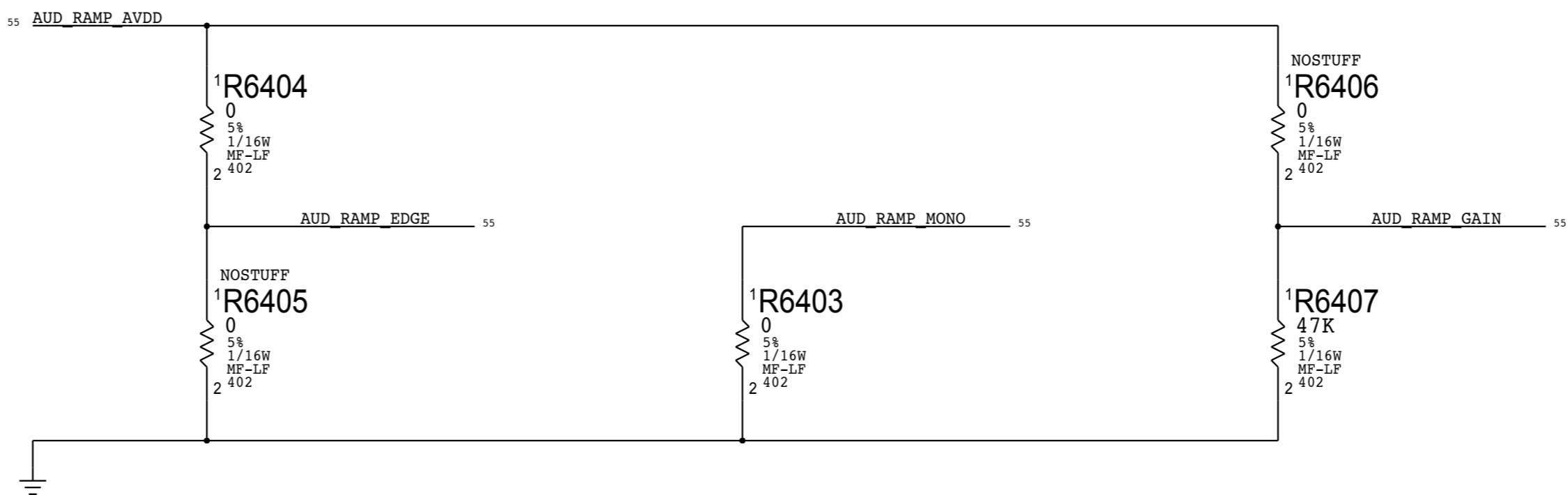
RIGHT CH SPEAKER AMP
APPLE P/N 353S3163

SPEAKER AMP GAIN = +12 DB
SPEAKER AMP RIN = 40K NOMINAL
FC_HPF, TWEETERS = ~847 HZ (4700 PF)
FC_HPF, WOOFERS = ~4 HZ (1.0 UF)

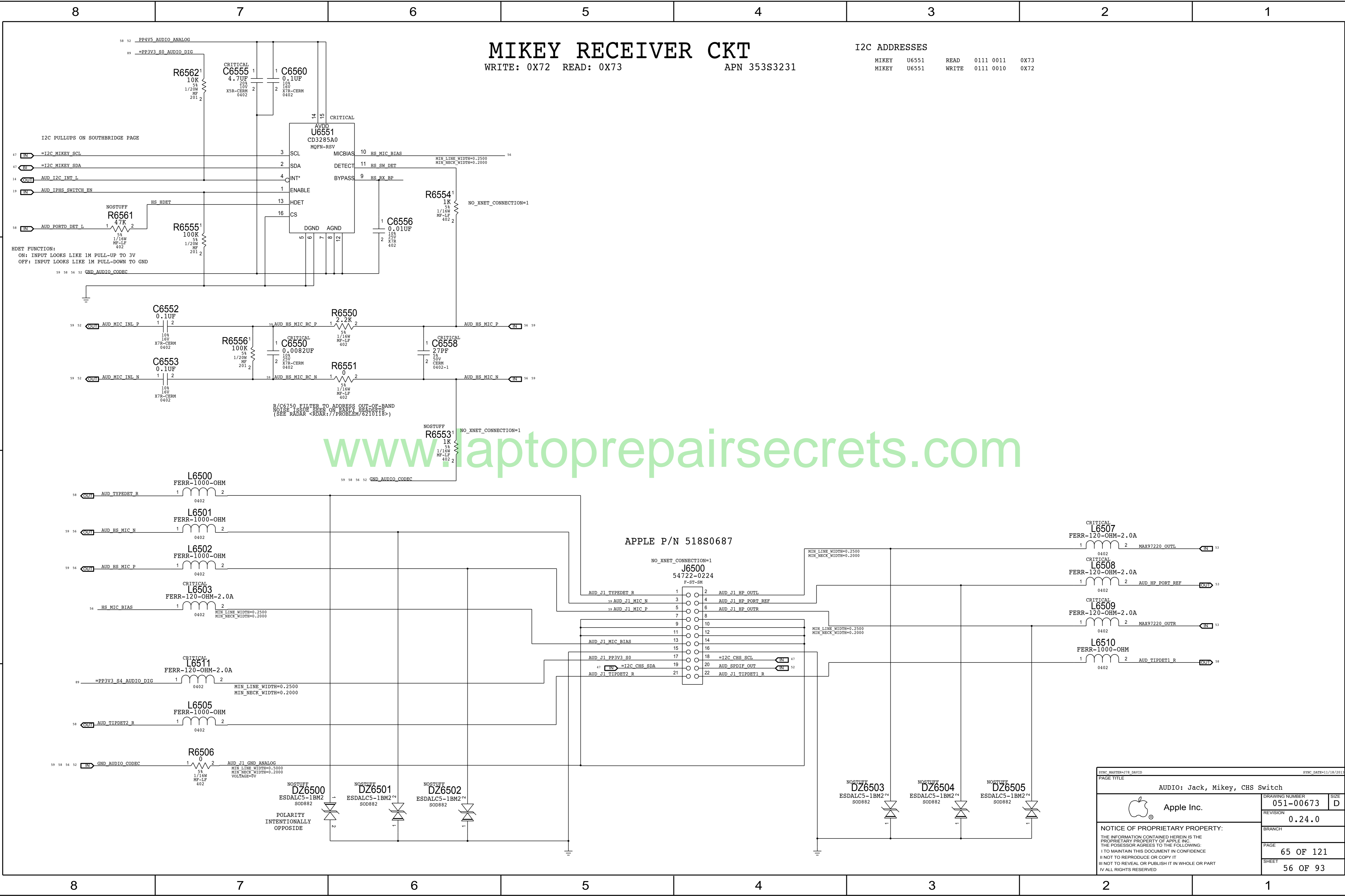


PINS 14 & 15 ARE TEST PINS AND
SHOULD BE TIED TO GND

EDGE RATE		GAIN	
CONTROL	R6404	+9 DB	R6406
ON	0 OHM	+12 DB	NOSTUFF
OFF	NOSTUFF	+15 DB	NOSTUFF
		+18 DB	NOSTUFF
		+24 DB	0 OHM
		AUD RAMP MONO NET:	
		HIGH = MONO OPERATION	
		LOW = STEREO OPERATION	

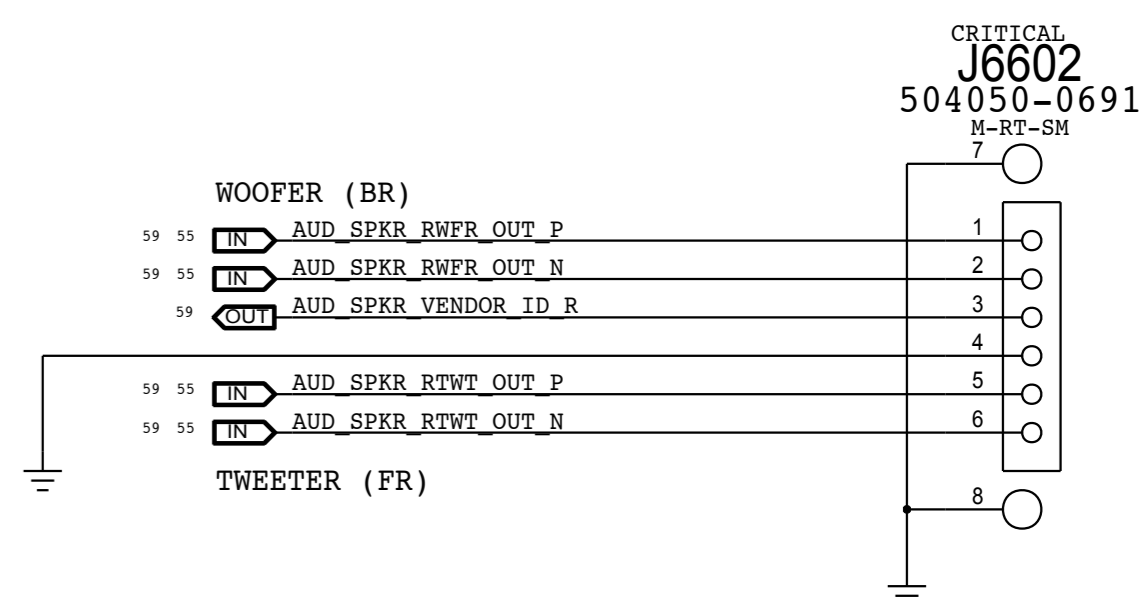
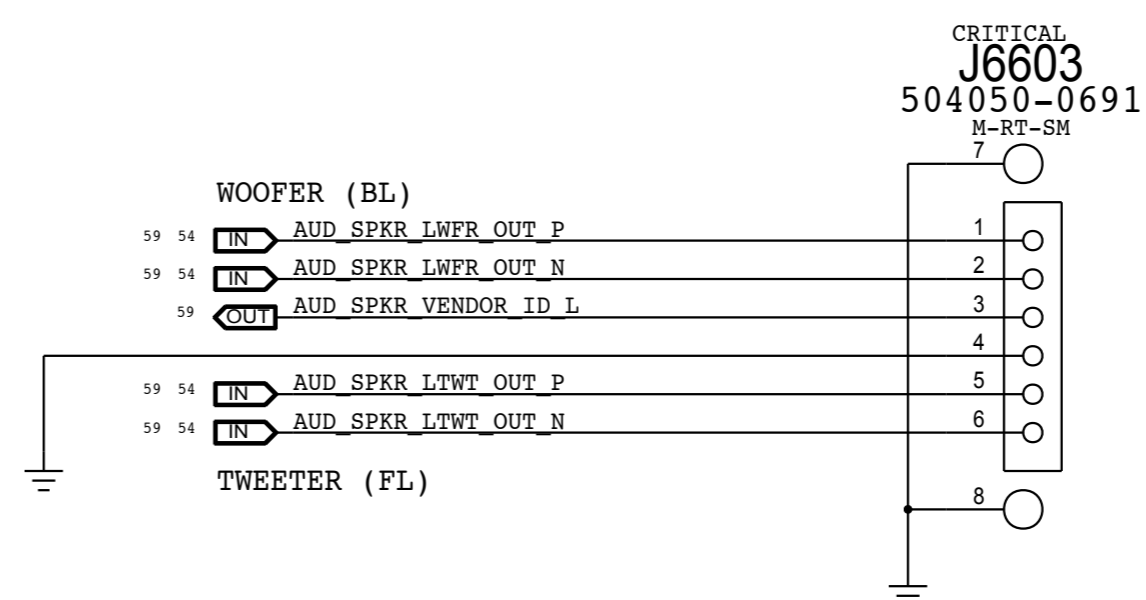


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PAGE TITLE					
AUDIO: RIGHT SPKR AMP					
		DRAWING NUMBER	051-00673		
		REVISION	0.24.0		
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		PAGE	64 OF 121		
		SHEET	55 OF 93		



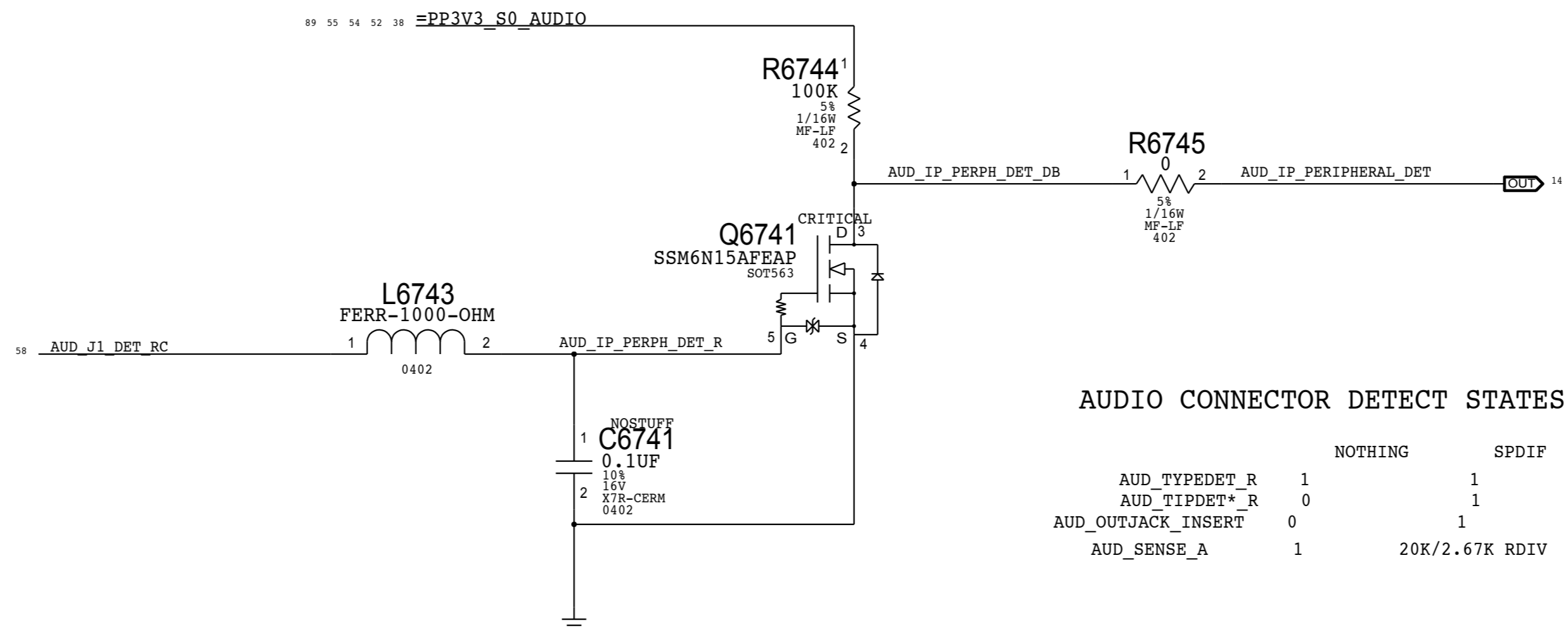
SPEAKER CABLE CONNECTORS

APPLE P/N 518S0862



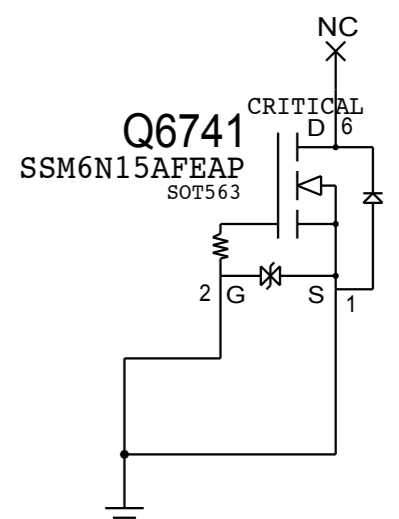
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IPHS HS Detect Debounce CKT

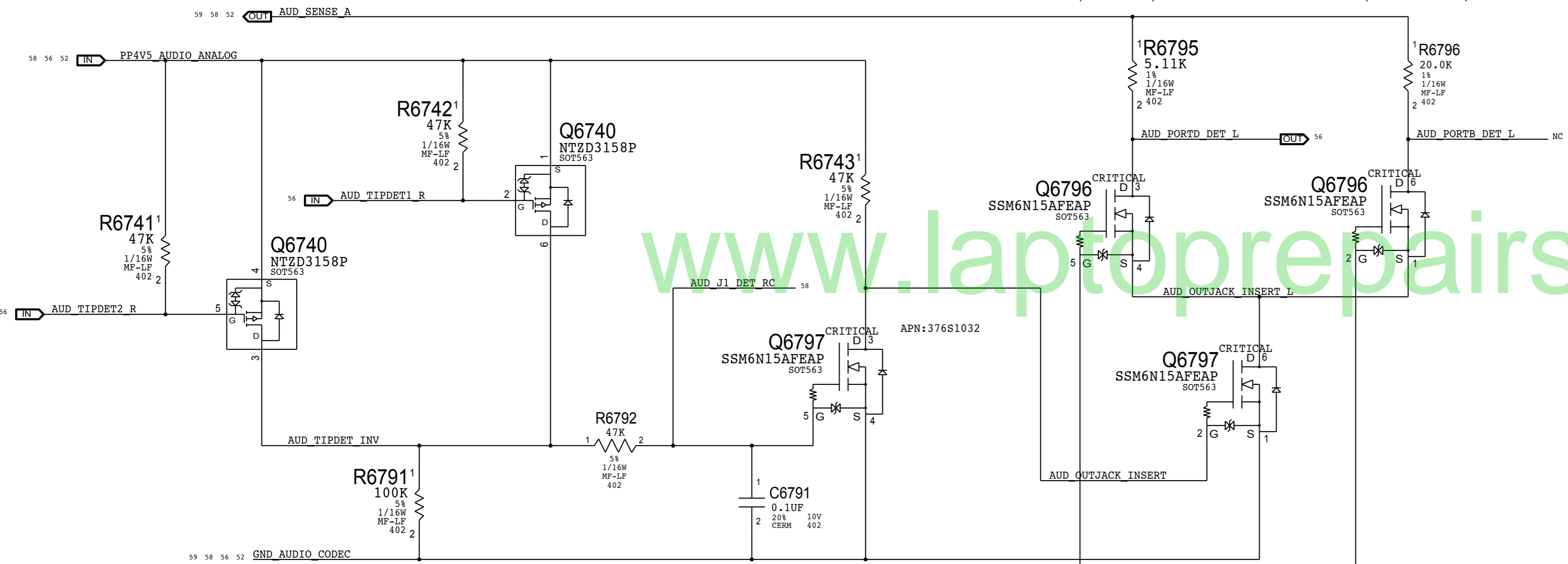


AUDIO CONNECTOR DETECT STATES

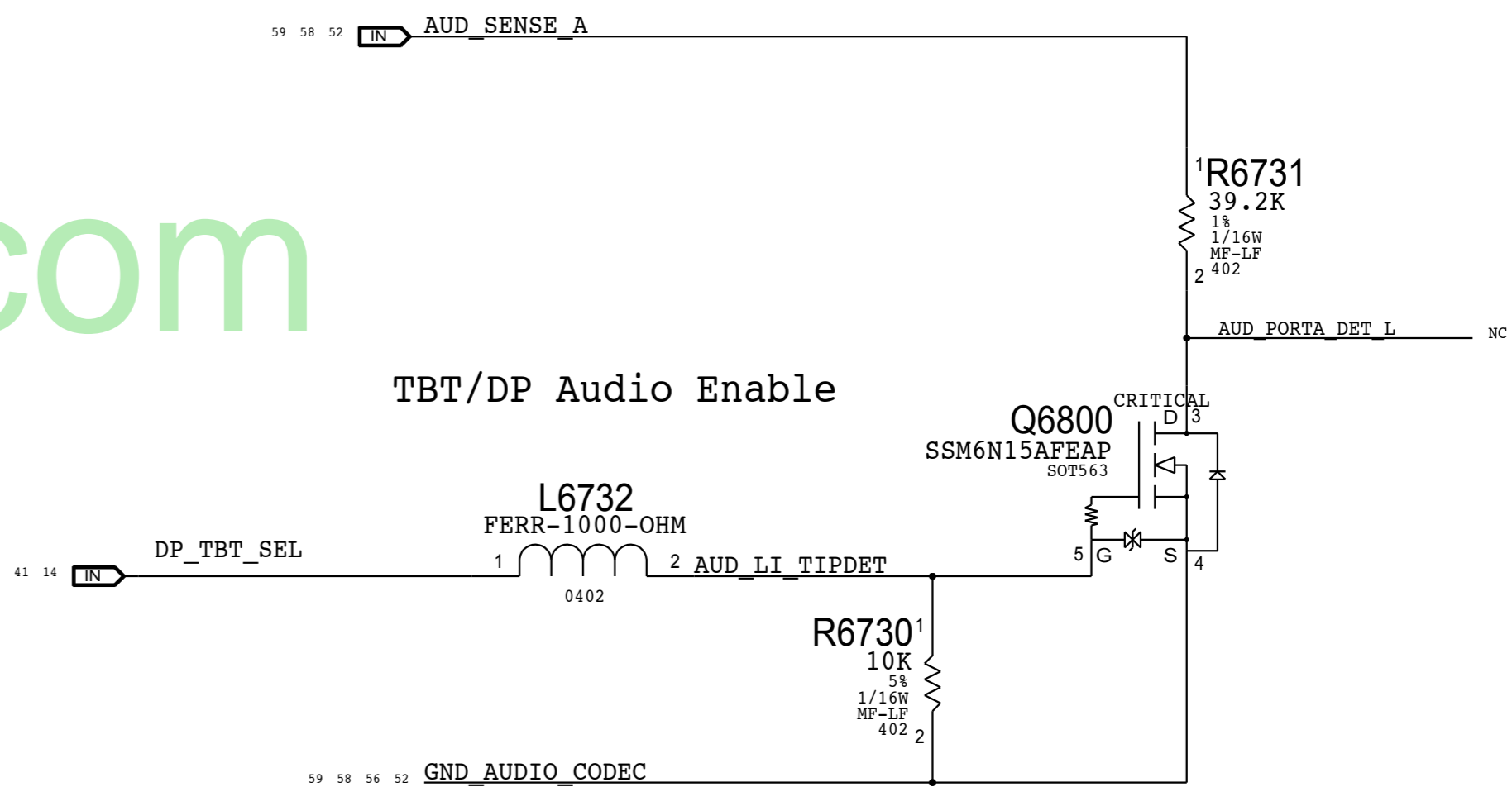
	NOTHING	SPDIF	HEADPHONE
AUD_TYDEDET_R	1	1	0
AUD_TIPDET*_R	0	1	1
AUD_OUTJACK_INSERT	0	1	1
AUD_SENSE_A	1	20K/2.67K RDIV	5.11K/2.67K RDIV



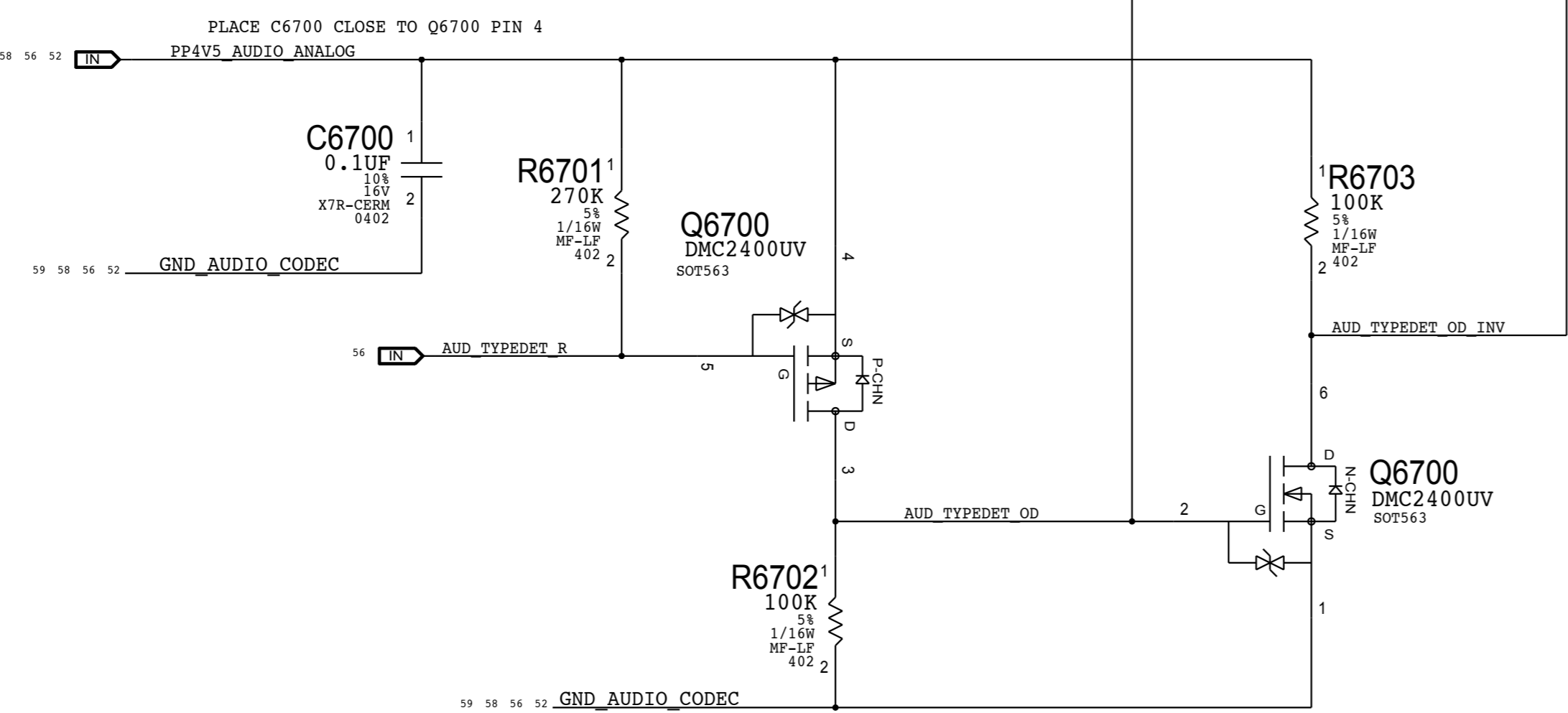
PORT D DETECT (HEADPHONES) PORT B DETECT (SPDIF DELEGATE)



Target Display Mode Detect



TBT/DP Audio Enable



D

C

B

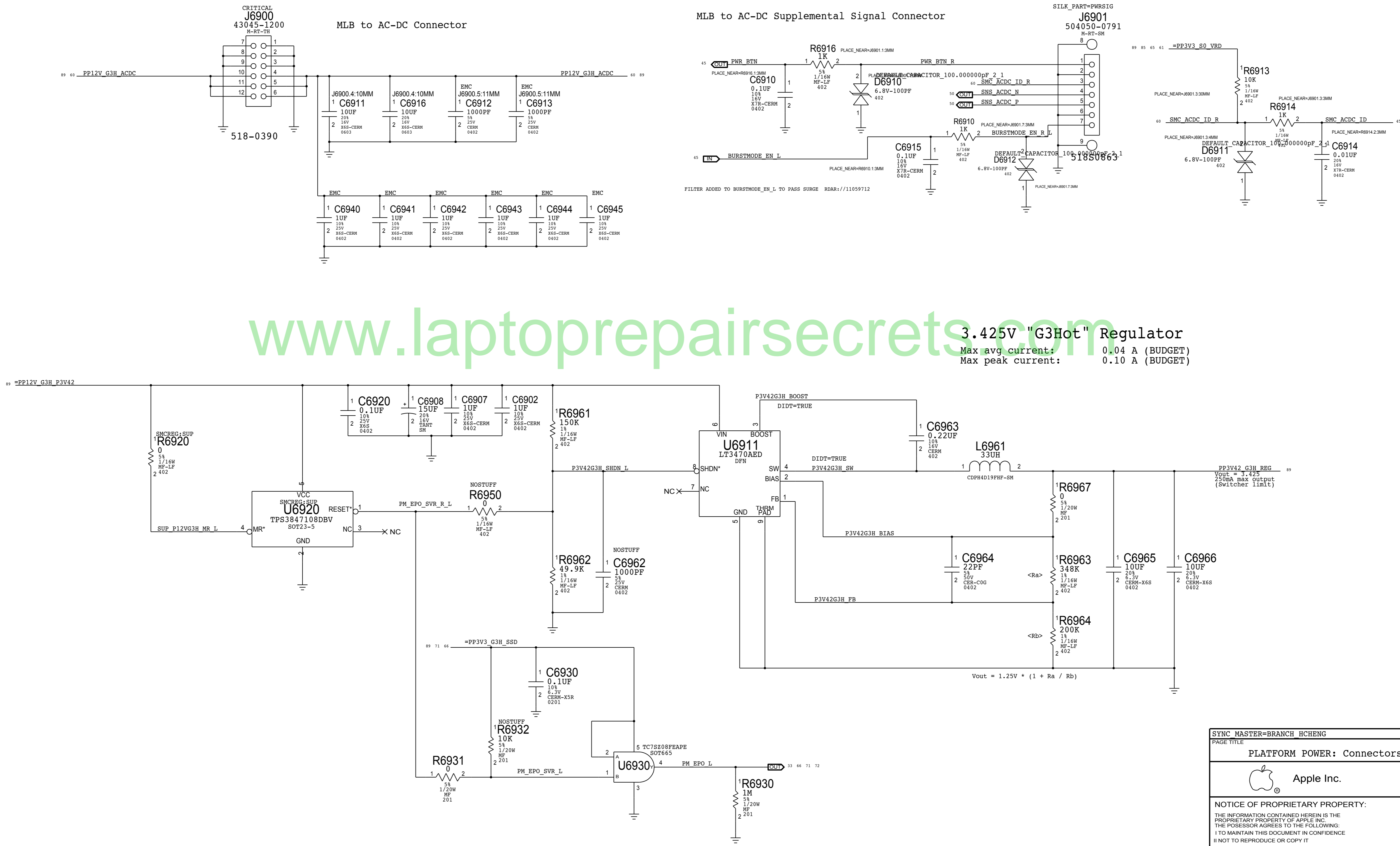
A


D

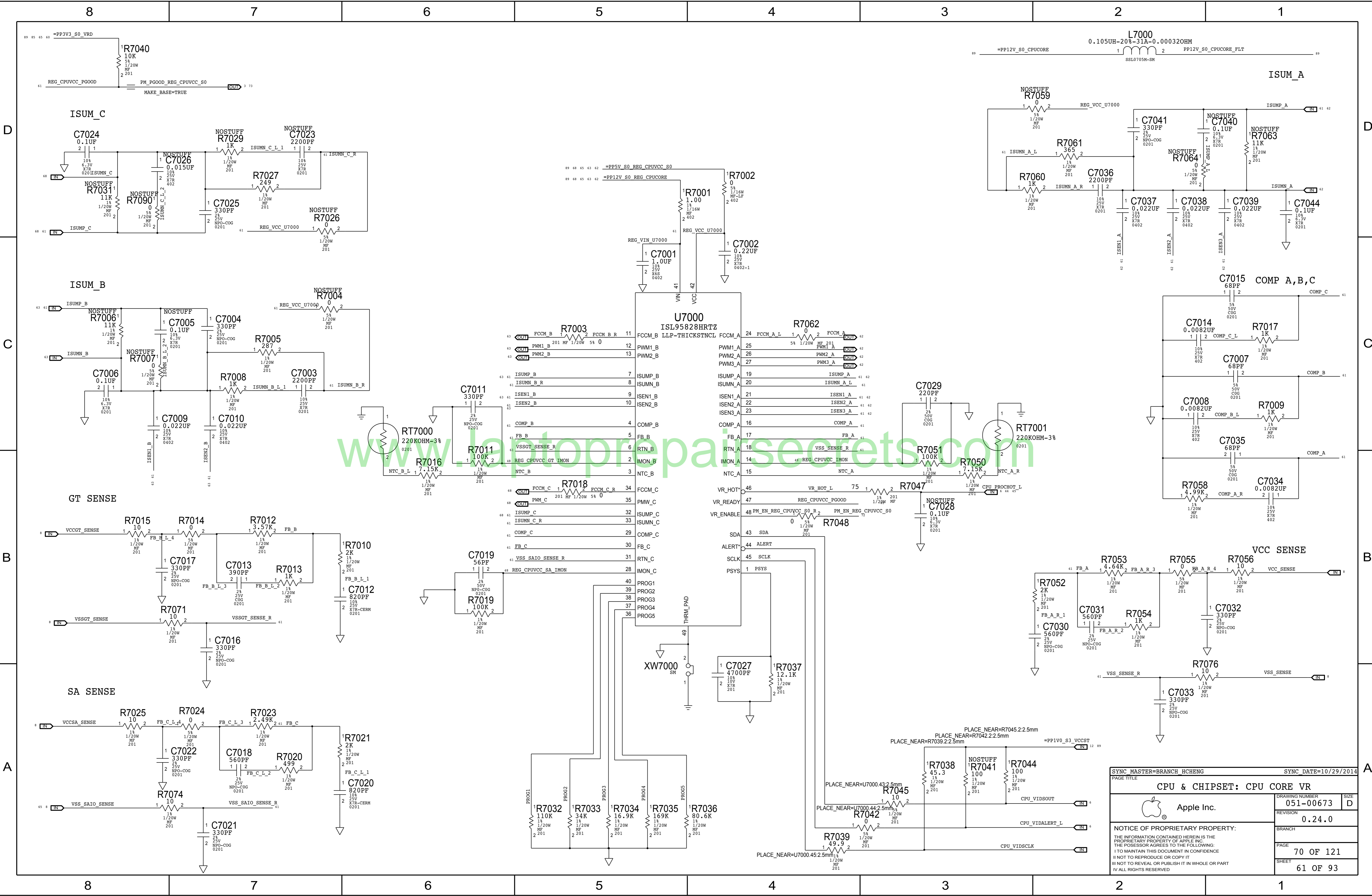
C


B

A



SYNC_MASTER=BRANCH HCHENG		SYNC_DATE=10/29/2014	
PAGE TITLE			
PLATFORM POWER: Connectors / VReg G3Hot			
 Apple Inc.	DRAWING NUMBER 051-00673		SIZE D
	REVISION 0.24.0		
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		PAGE 69 OF 121	
		SHEET 60 OF 93	



SYNC_MASTER=BRANCH HCHENG		SYNC_DATE=10/29/2014	
PAGE TITLE			
CPU & CHIPSET: CPU CORE VR			
 Apple Inc.	DRAWING NUMBER		SIZE
	051-00673		D
	REVISION		
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		BRANCH	
		PAGE	
		70 OF 121	
		SHEET	
		61 OF 93	

CPU VCC Regulator
EDC = 100A
TDC = 70A

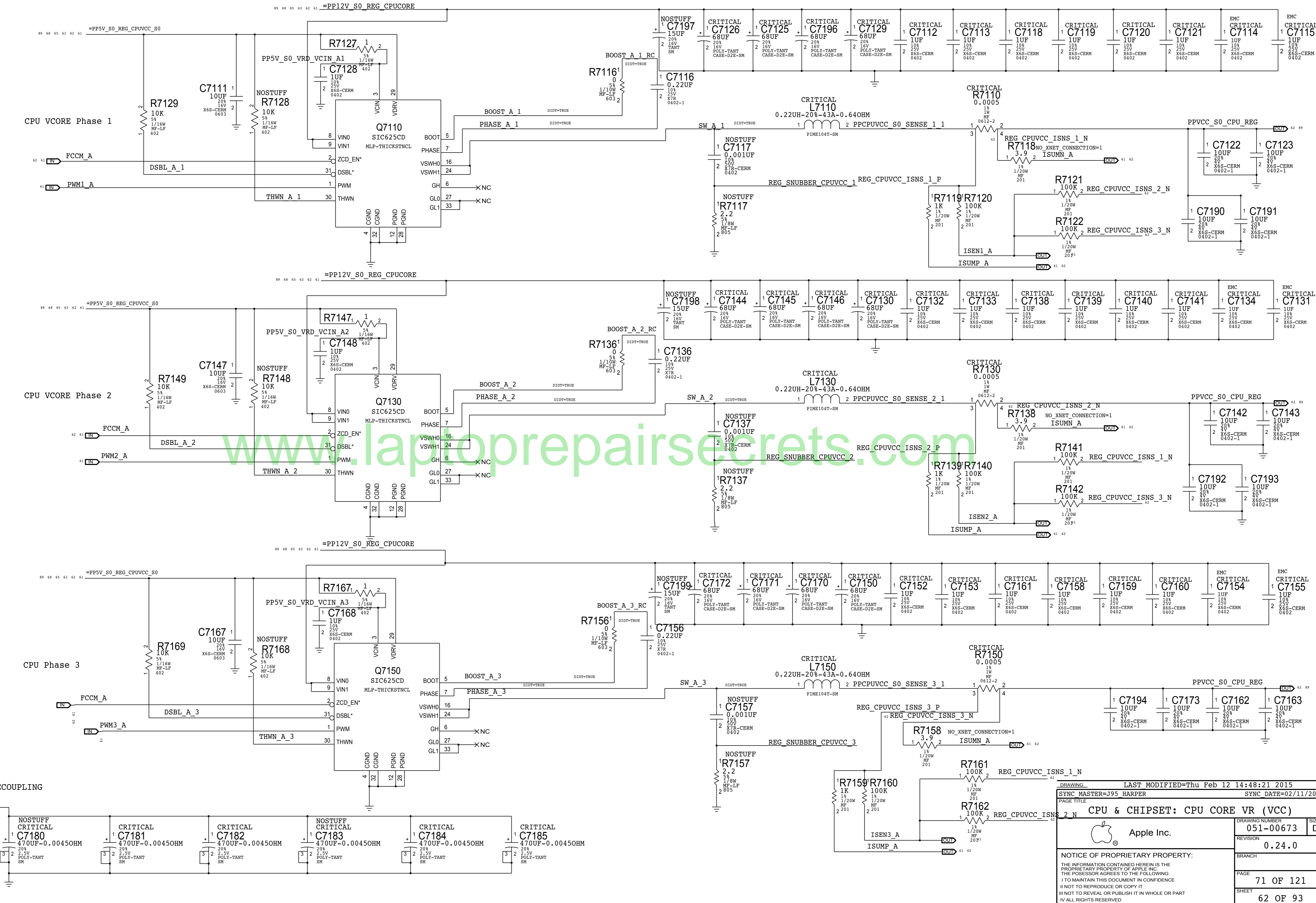
CPU VCORE Phase 1

CPU VCORE Phase 2

CPU Phase 3

CPU VCORE OUTPUT DECOUPLING

PPVCC_S0_CPU_REG



DRAWING		LAST MODIFIED=Thu Feb 12 14:48:21 2015	
SYNC MASTER=J95 HARPER		SYNC DATE=02/11/2015	
PAGE TITLE			
CPU & CHIPSET: CPU CORE VR (VCC)			
DRAWING NUMBER		051-00673	
REVISION		0.24.0	
BRANCH			
PAGE		71 OF 121	
SHEET		62 OF 93	

D

C

R


Δ



C

B

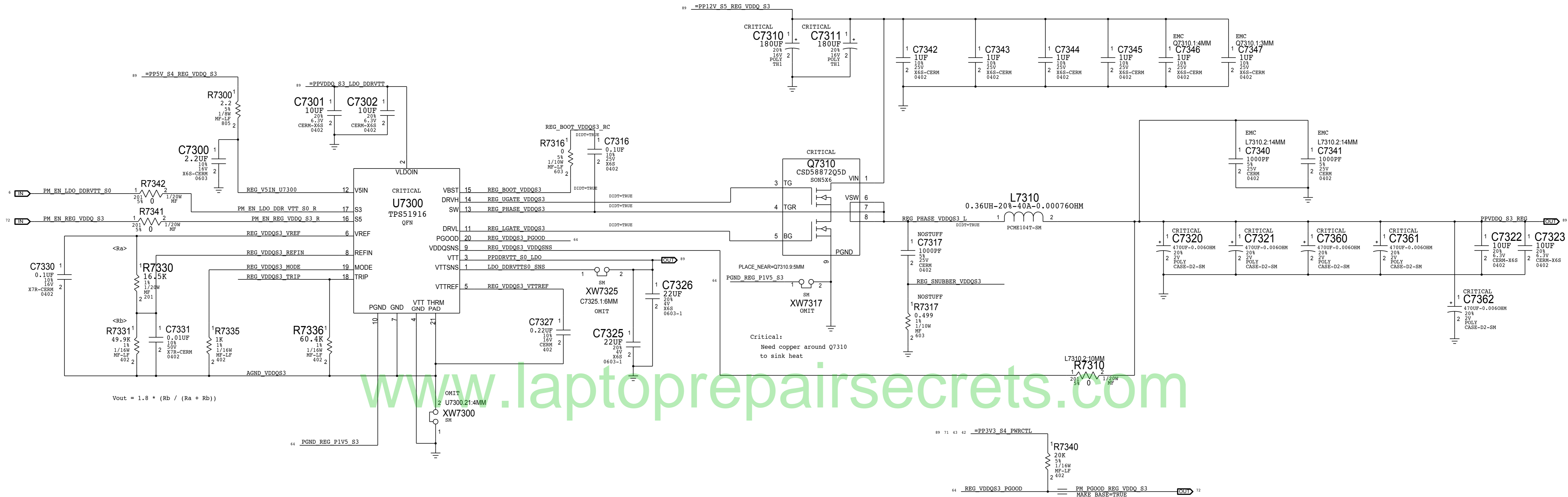
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DRAWING _____		LAST MODIFIED=Thu Feb 12 14:48:21 2015	
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PAGE TITLE			
CPU & CHIPSET: CPU CORE VR (VCCGT)			
	Apple Inc.		SIZE
	051-00673		D
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		BRANCH	
		PAGE	72 OF 121
		SHEET	63 OF 93

VDDQ (1.35V) S3 REGULATOR

EDC = 20A

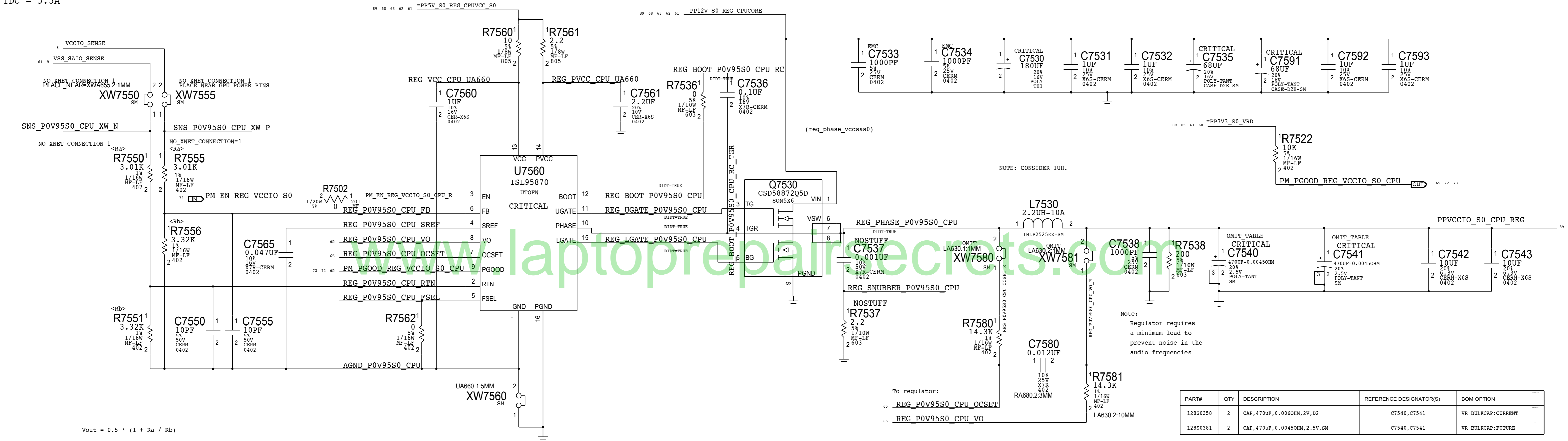
TDC = 14A




VCCIO (0.95V) S0 REGULATOR

EDC = 5.5A

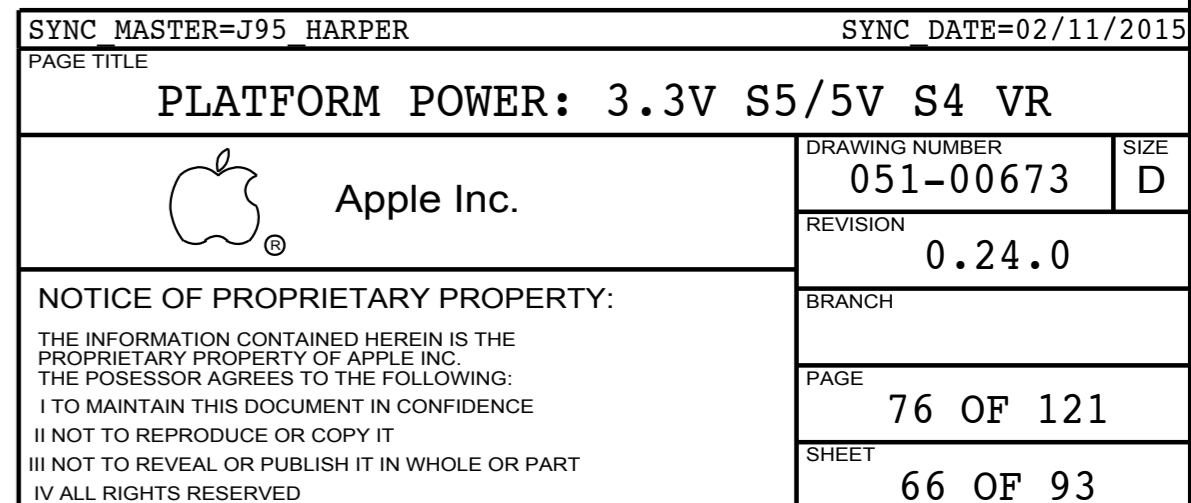
TDC = 5.5A



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CPU & CHIPSET: CPU VCCIO VR			
 Apple Inc.	DRAWING NUMBER		SIZE
	051-00673		D
	REVISION		0.24.0
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		75 OF 121	
		SHEET	
		65 OF 93	

EDC = 12.46A
TDC = 9.4A

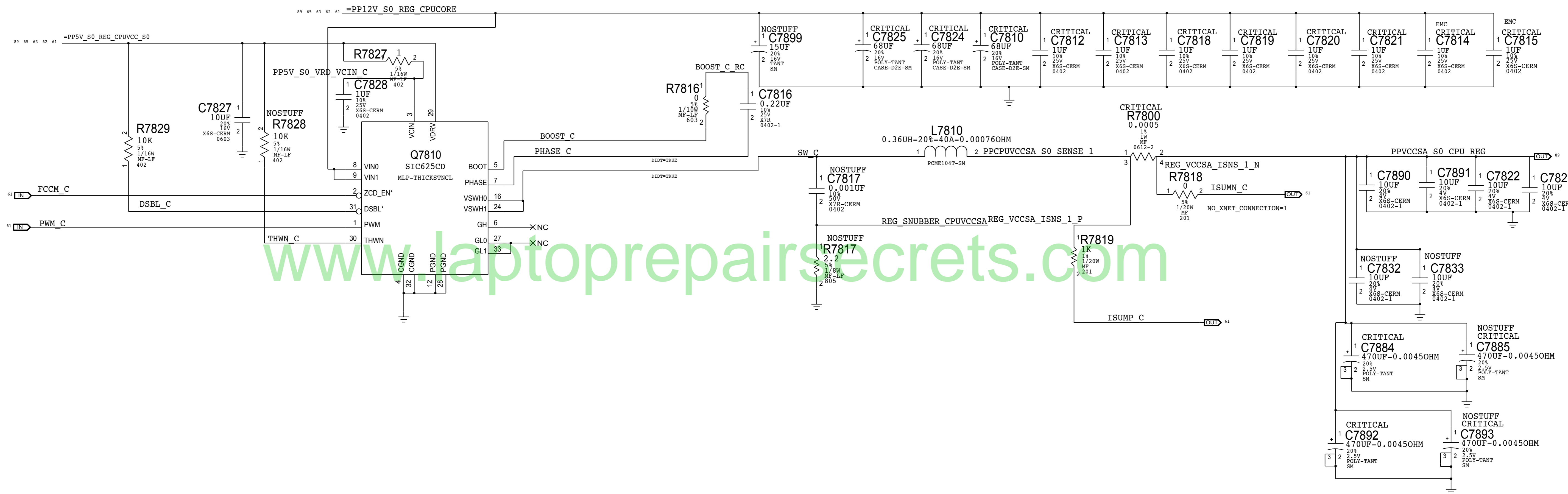
EDC = 6.5A
TDC = 5.9A




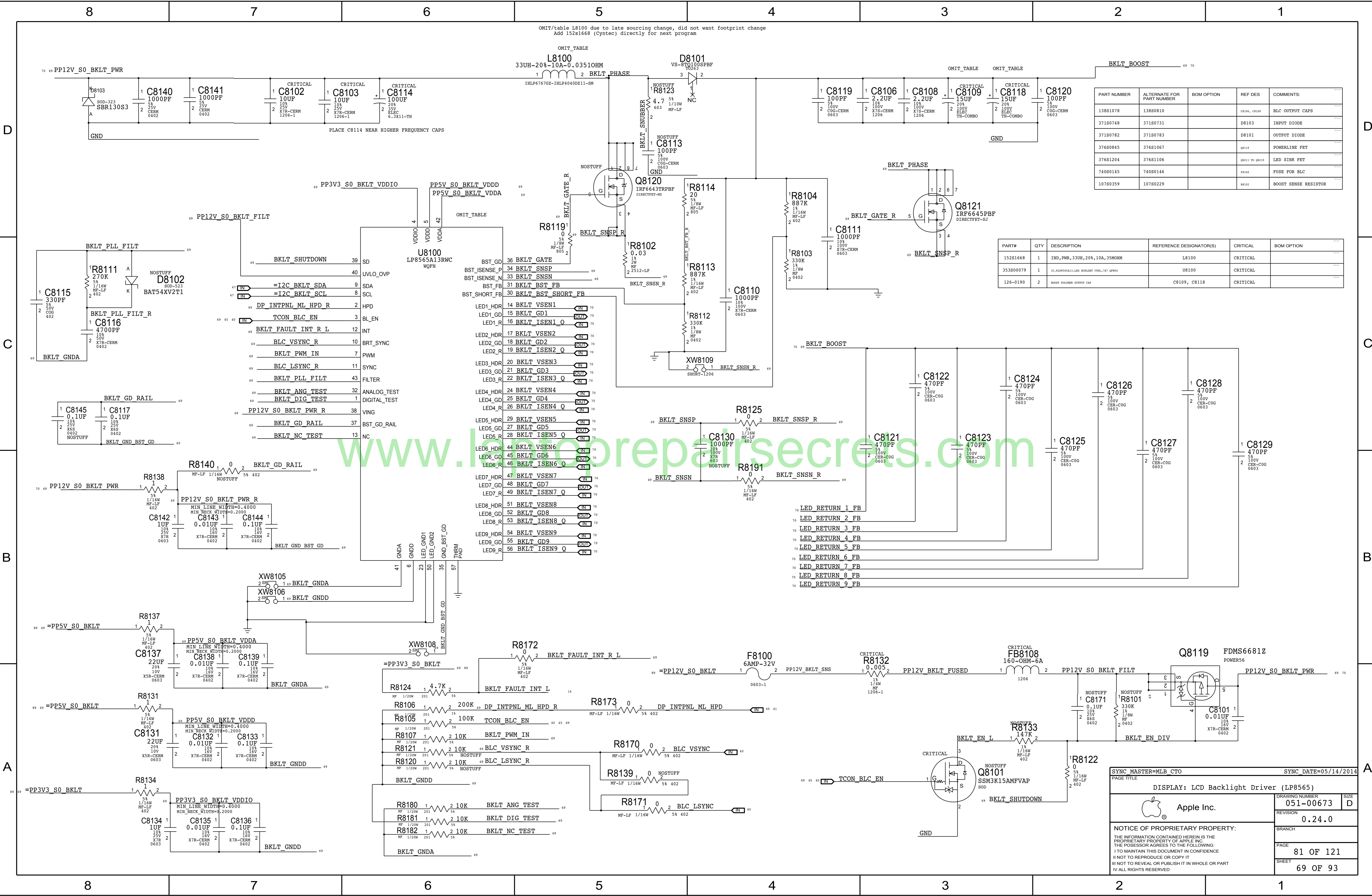
CPU VCCSA Regulator

EDC = 11.1A

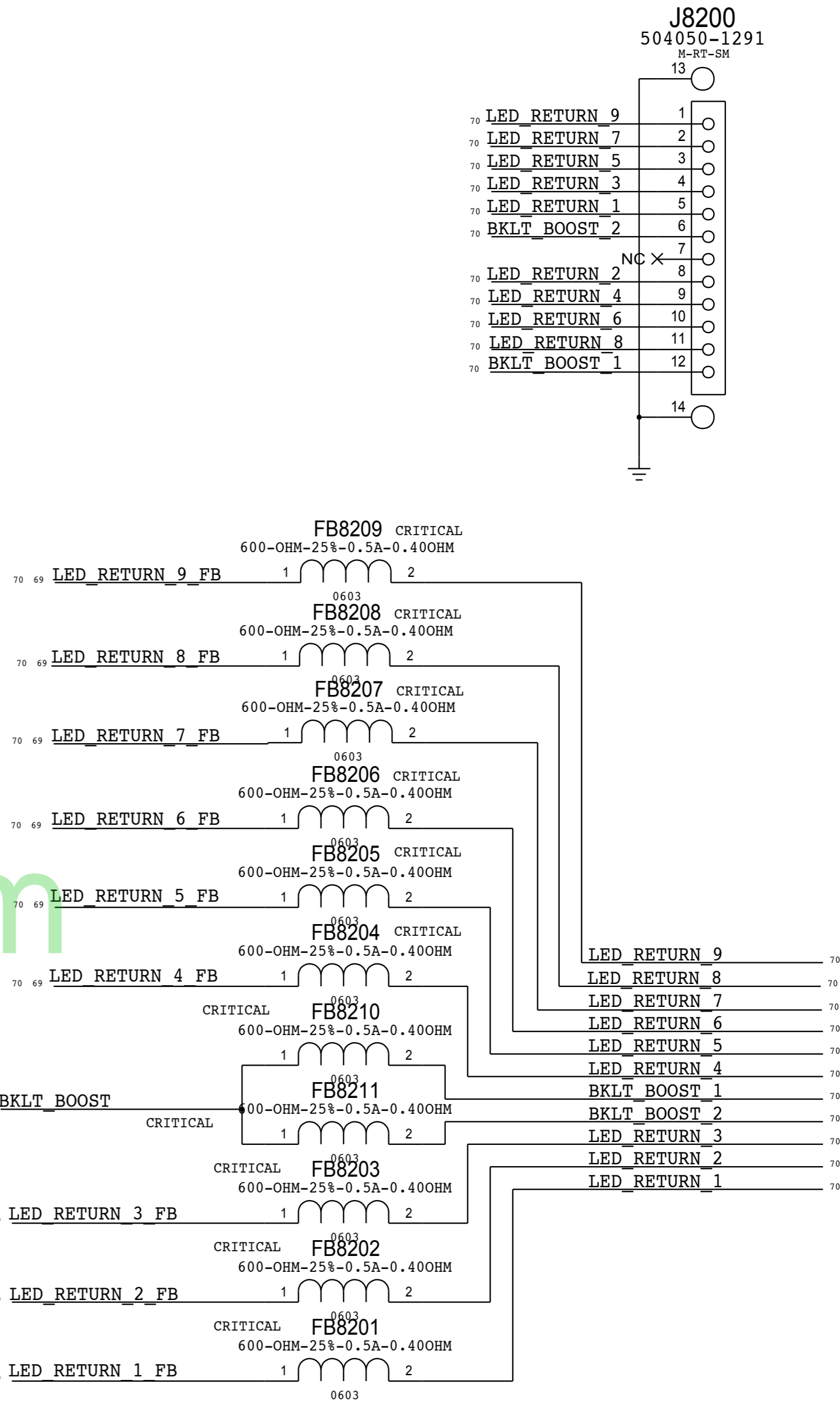
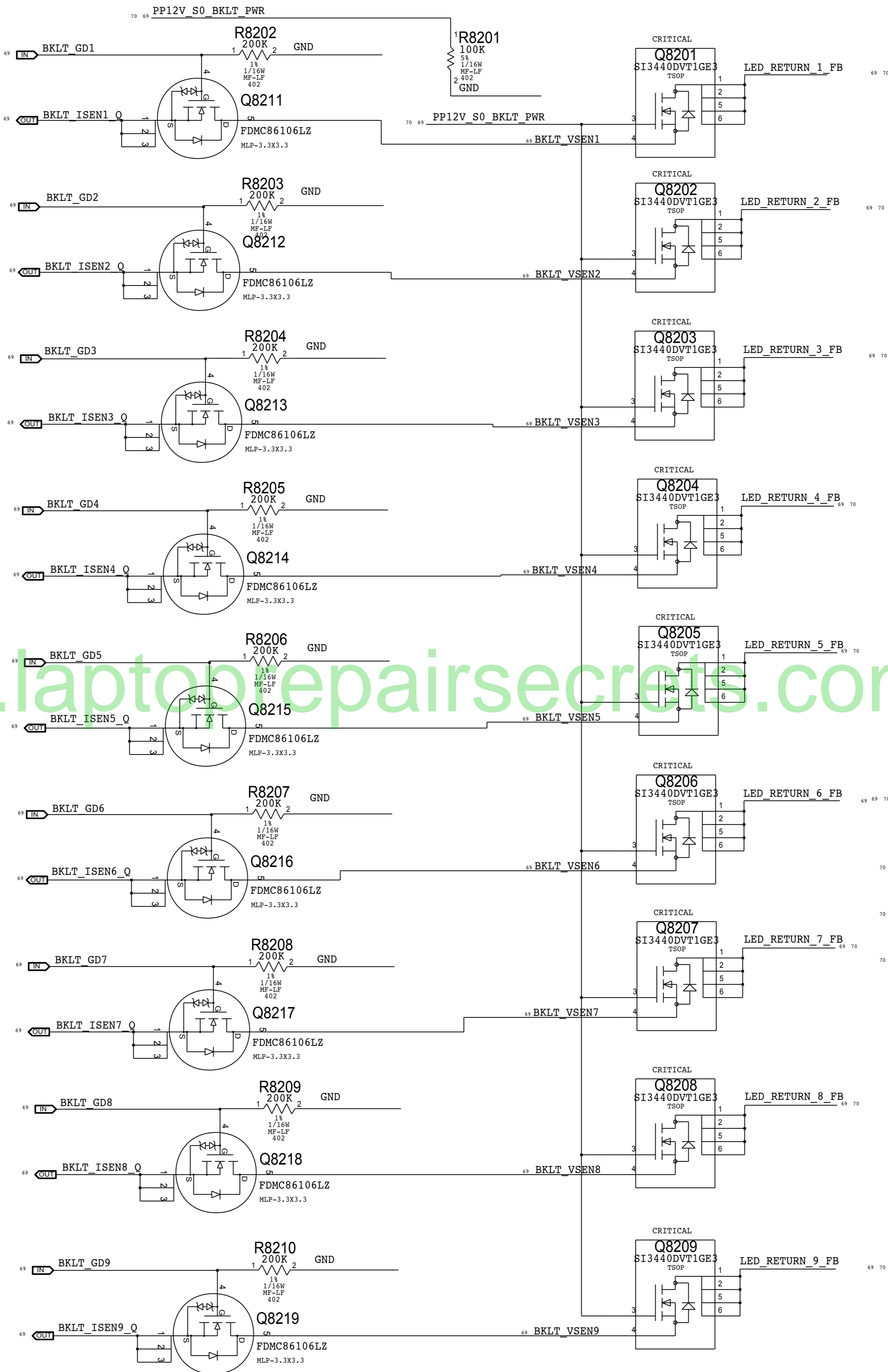
TDC = 10A




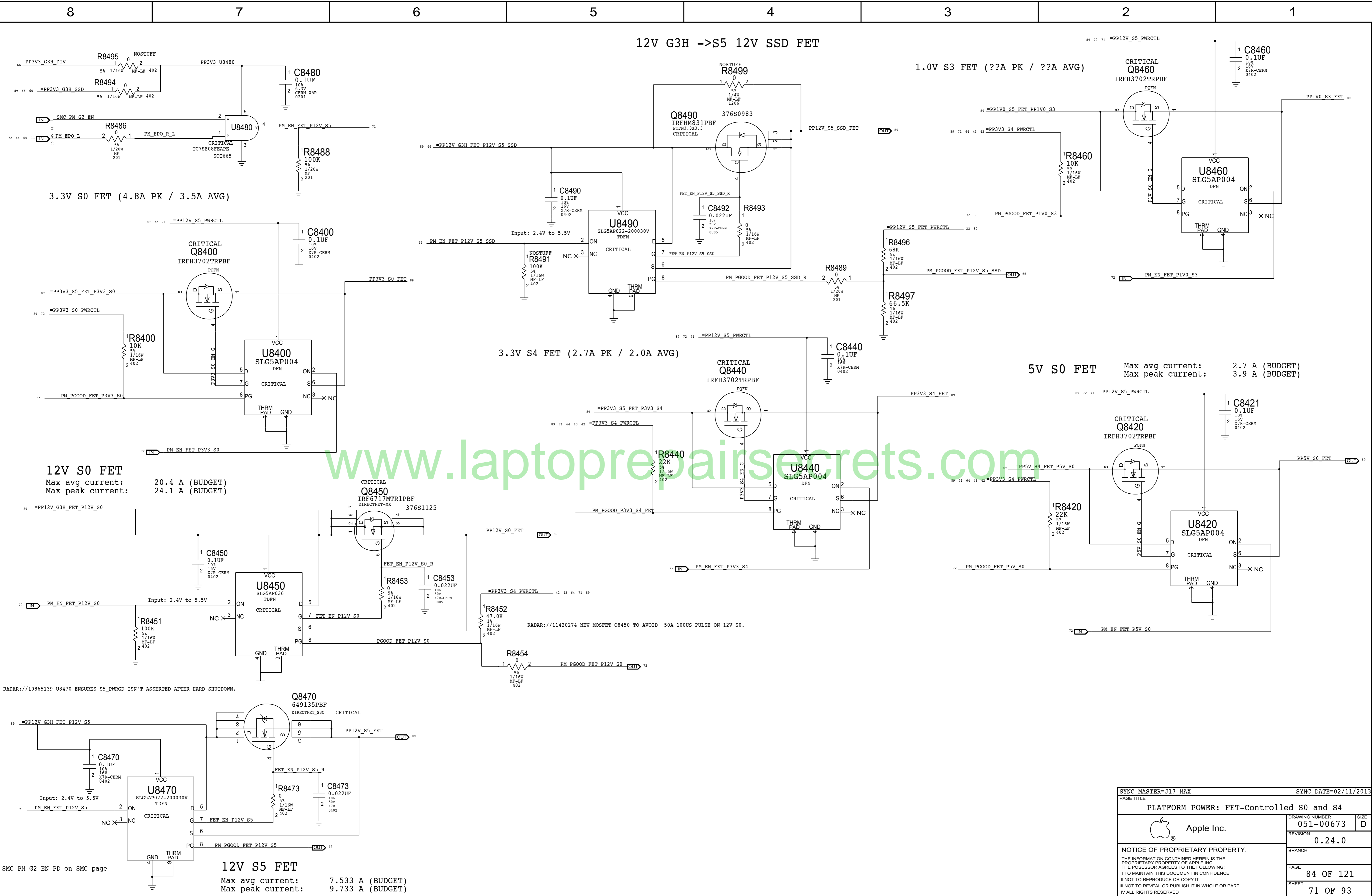
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SYNC MASTER=J95 HARPER		SYNC DATE=02/11/2015	
PAGE TITLE			
CPU & CHIPSET: CPU CORE VR (VCCSA)			
 Apple Inc. ®		DRAWING NUMBER	051-00673
		REVISION	0.24.0
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		PAGE	78 OF 121
		SHEET	68 OF 93



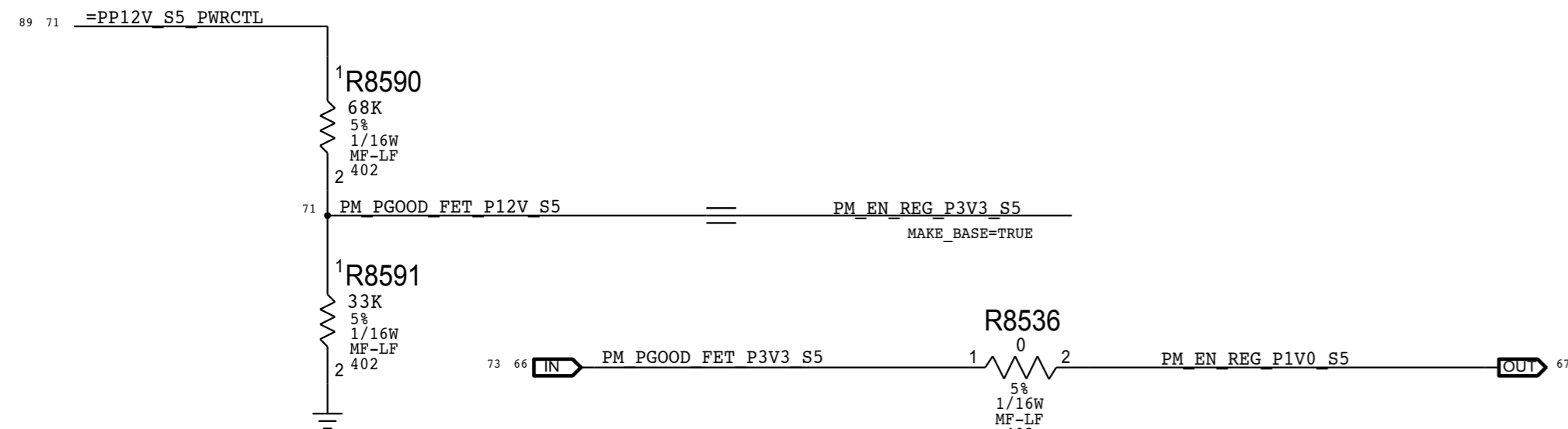
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S1256	376S1073		ALL	Short Protection FET
155S0831	155S0797		ALL	FB8201 TO FB8211



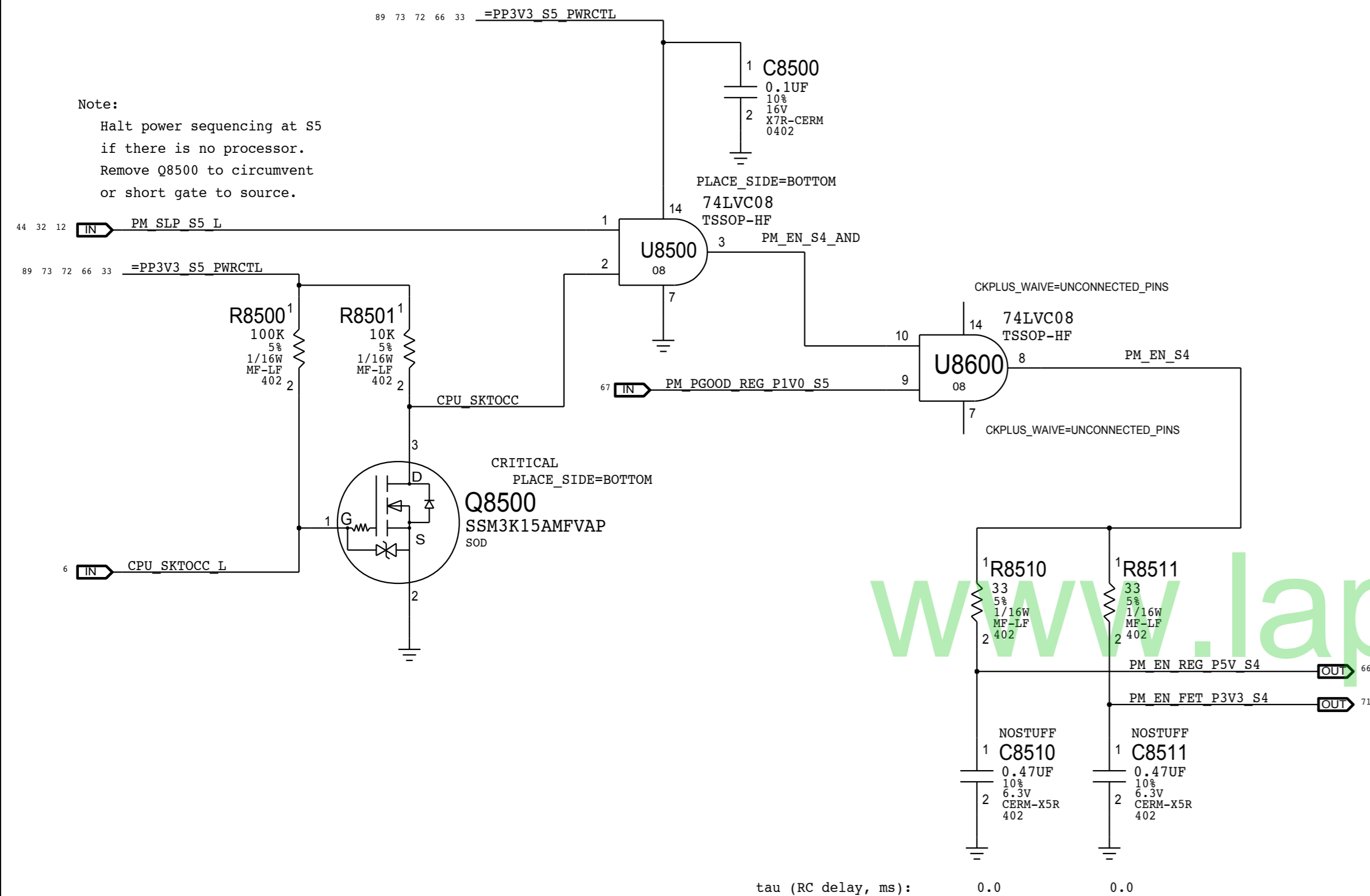
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PAGE TITLE					
DISPLAY: Backlight Driver 2					
 Apple Inc.		DRAWING NUMBER	051-00673	SIZE	D
		REVISION	0.24.0		
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		PAGE			
		SHEET			
		82 OF 121			
		70 OF 93			



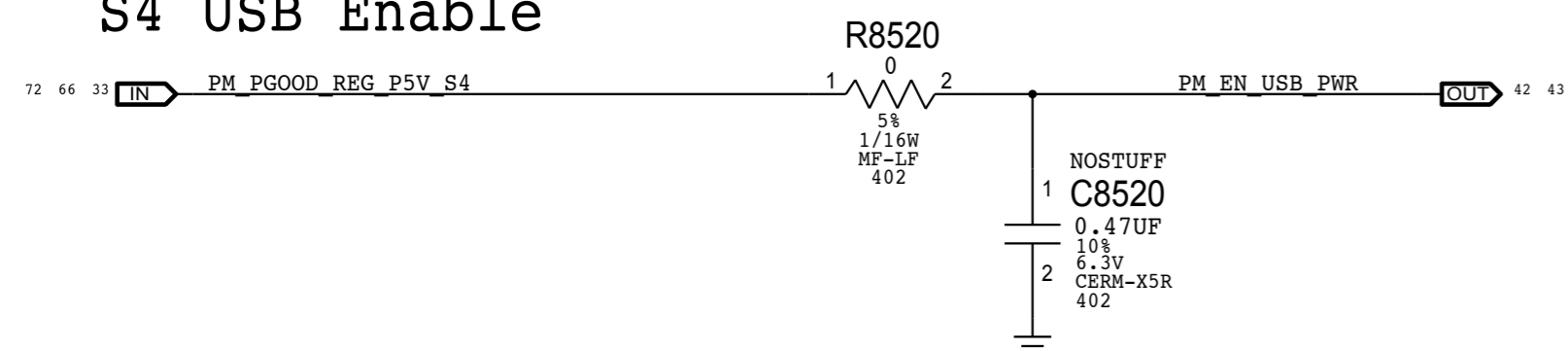
S5 Enable



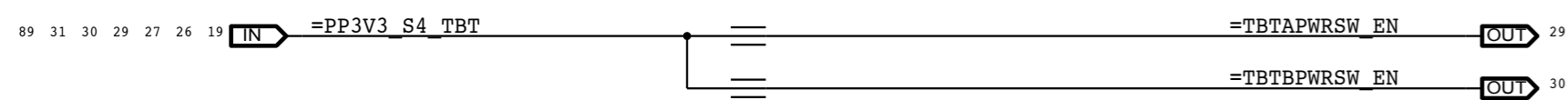
S4 Enables



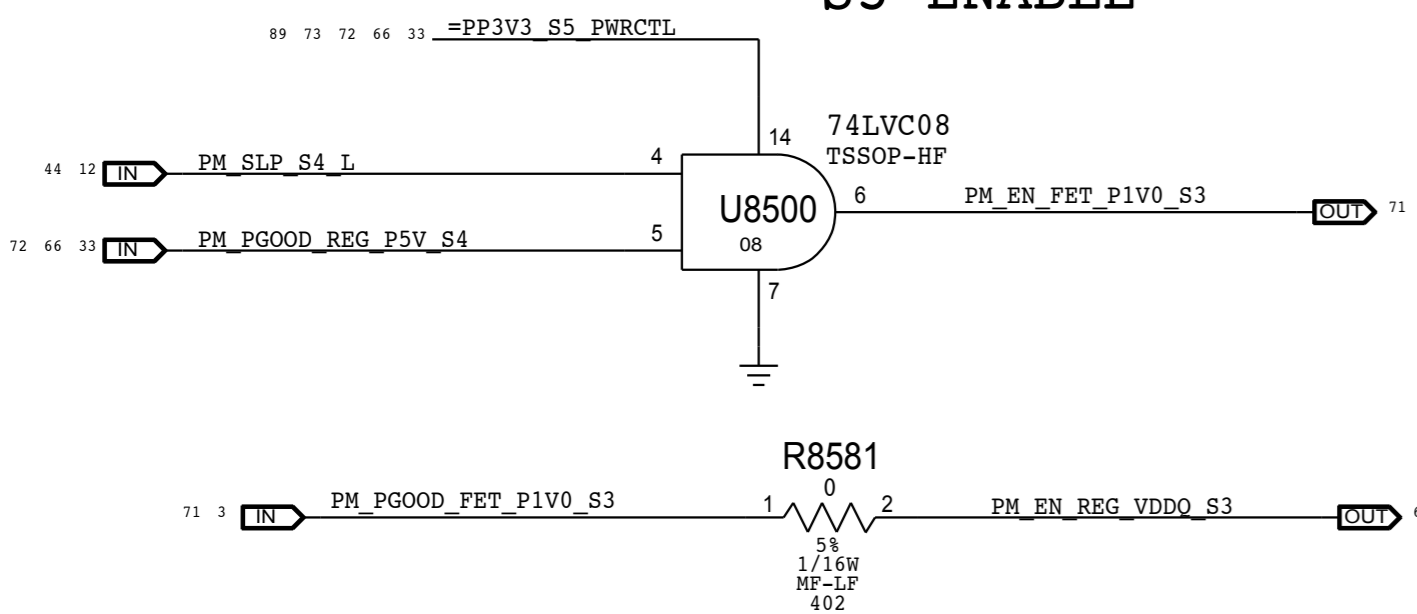
S4 USB Enable



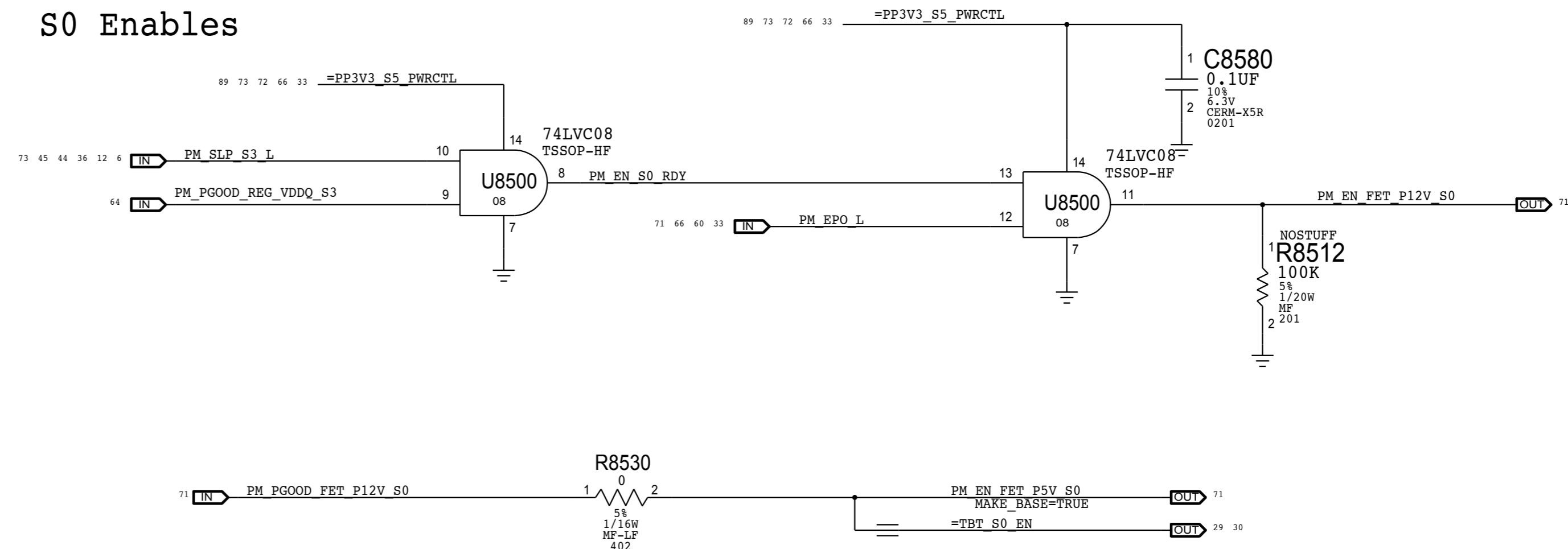
S4 TBT S4 Port Enable



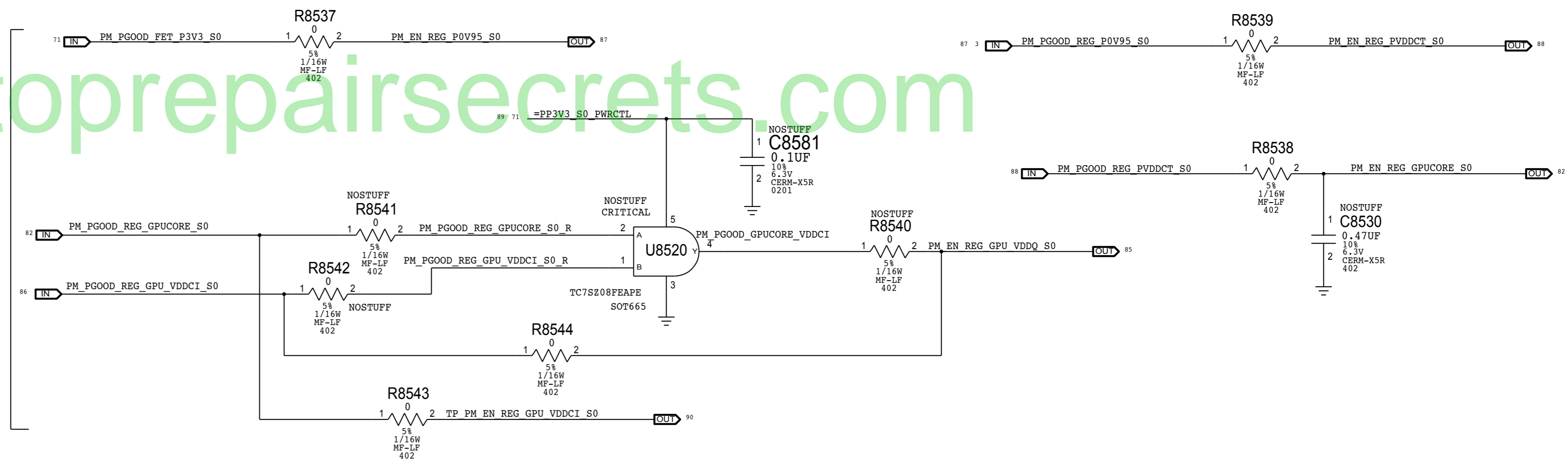
S3 ENABLE



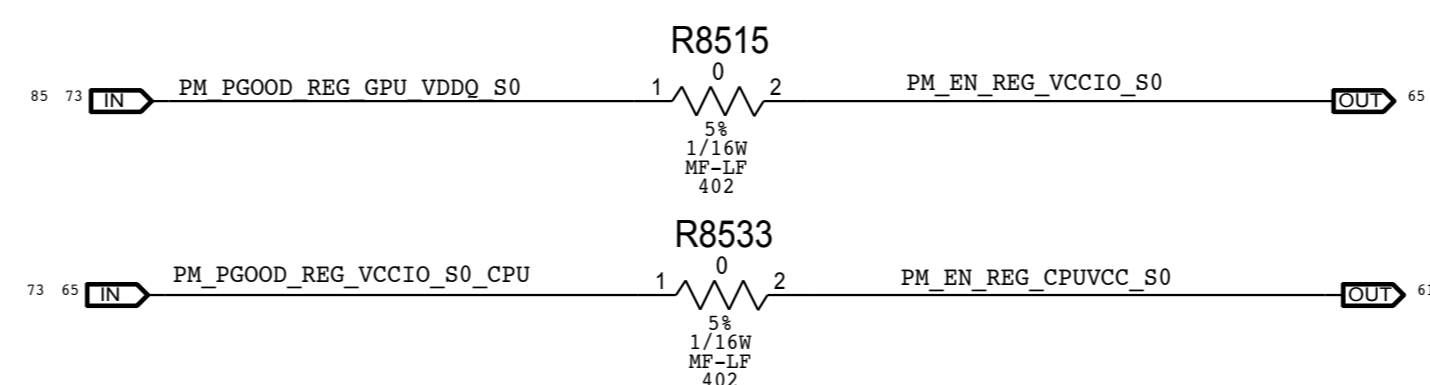
S0 Enables



S0 GPU SEQUENCING



S0 CPU Sequencing



Power Sequencing requirements

System:


- ```

1. 12V_ADCCD -> 3V42G3H -> 12V_S5/12V_S5_SSD -> 3V3_S5 -> 1V0_S5 -> 5V_S4/3V3_S4 -> 1V0_S3

Intel CPU:
2. 1V0_S3 -> VDDQ_S3 -> 12V_S0 -> 5V_S0 -> 3V3_S0 -> GPU Rails -> VCCIO_S0-> VCC_CPU_S0 (VCCGT & VCCSA)

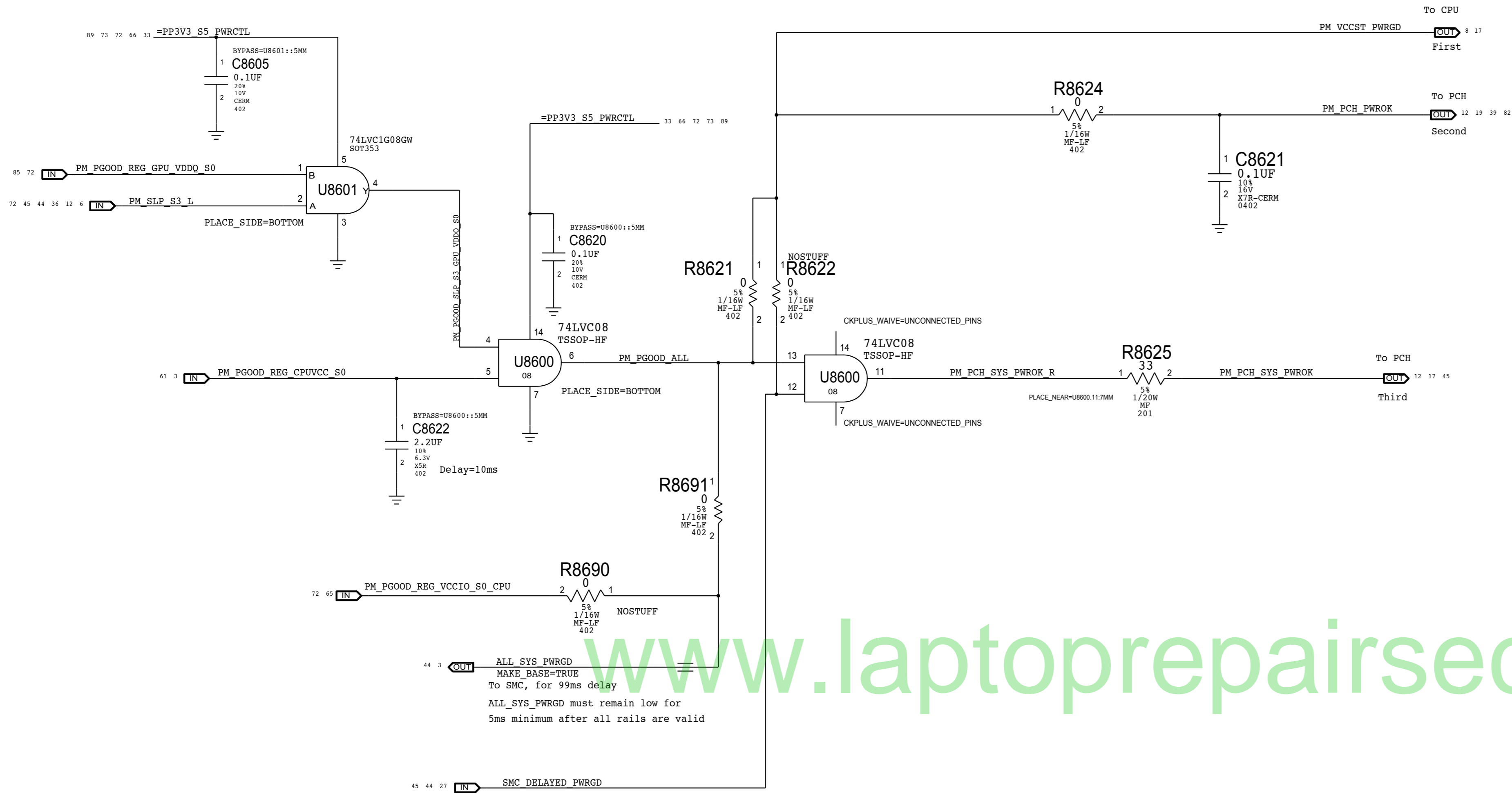
AMD GPU:
3. 3V3_S0 -> 0V95 -> 1V8 (VDD_CT) -> GPUCORE (VDDC) -> VDDCI -> FBVDDQ

```

|                                                                                                                                                                                                                                                                                      |                |                      |      |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------|----------------------|------|
| SYNC MASTER=J78 KENNY                                                                                                                                                                                                                                                                |                | SYNC DATE=12/18/2013 |      |
| PAGE TITLE                                                                                                                                                                                                                                                                           |                |                      |      |
| PLATFORM POWER: Regulator Enables                                                                                                                                                                                                                                                    |                |                      |      |
|  Apple Inc.                                                                                                                                                                                     | DRAWING NUMBER |                      | SIZE |
|                                                                                                                                                                                                                                                                                      | 051-00673      |                      | D    |
|                                                                                                                                                                                                                                                                                      | REVISION       |                      |      |
|                                                                                                                                                                                                                                                                                      | 0.24.0         |                      |      |
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|                                                                                                                                                                                                                                                                                      |                | 85 OF 121            |      |
|                                                                                                                                                                                                                                                                                      |                | SHEET                |      |
|                                                                                                                                                                                                                                                                                      |                | 72 OF 93             |      |

ALL\_SYS\_PWRGD,PCH\_PWROK & SYS\_PWROK Generation

PCH Power Goods



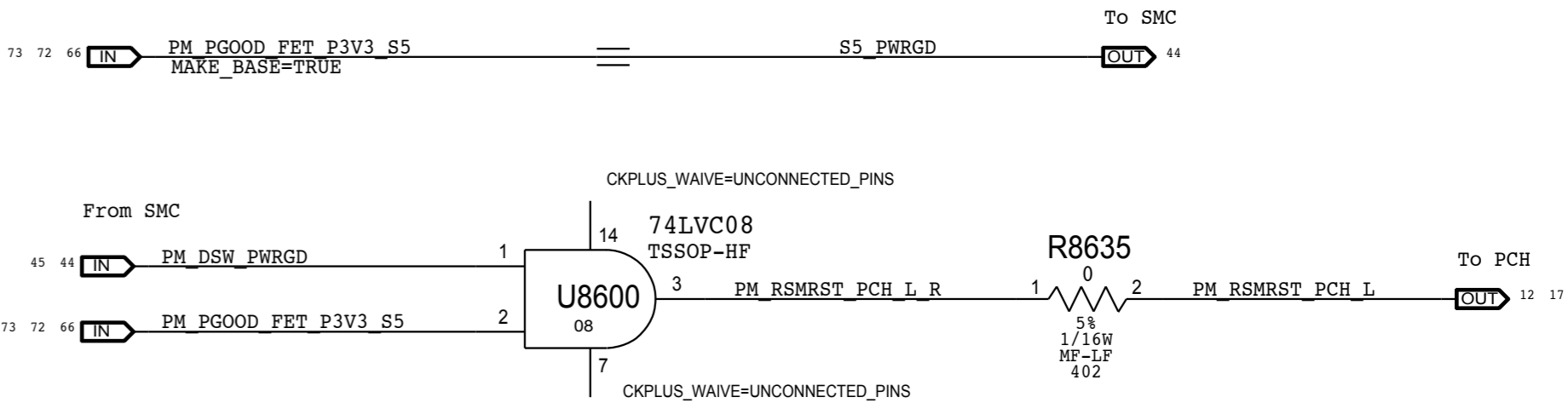
Resume Reset

Intel Doc# 29517 Maho Bay PDG, Section 22.13  
Intel Doc# 29562 Panther Point EDS, Section 8.7 and 8.8

Note:  
THE IMAC J78 DESIGNS DOES NOT SUPPORT DEEP SX MODES SO BOTH DPWROK AND RSMRST# signals are shorted together

Requirements:  
Power on:  
    Asserted at least 10 ms after all suspend well power is valid  
Power off or loss of AC:  
    Transition to 0.8V or less before VccSUS3\_3 drops to 2.90 V  
    to allow PCH to switch suspend well to battery without excessive loading

Method:  
The SMC guarantees proper assertion and de-assertion of RSMRST# for normal operation via PM\_DSW\_PWRGD.  
RSMRST# is asserted when power good from regulator is de-asserted in the event AC is lost. Power good de-assertion should happen quickly enough to meet Intel spec.



## Page Notes

Power aliases required by this page

- \*??771)\_GPO\_VCO1)

Signal aliases required by this pop

(1992).

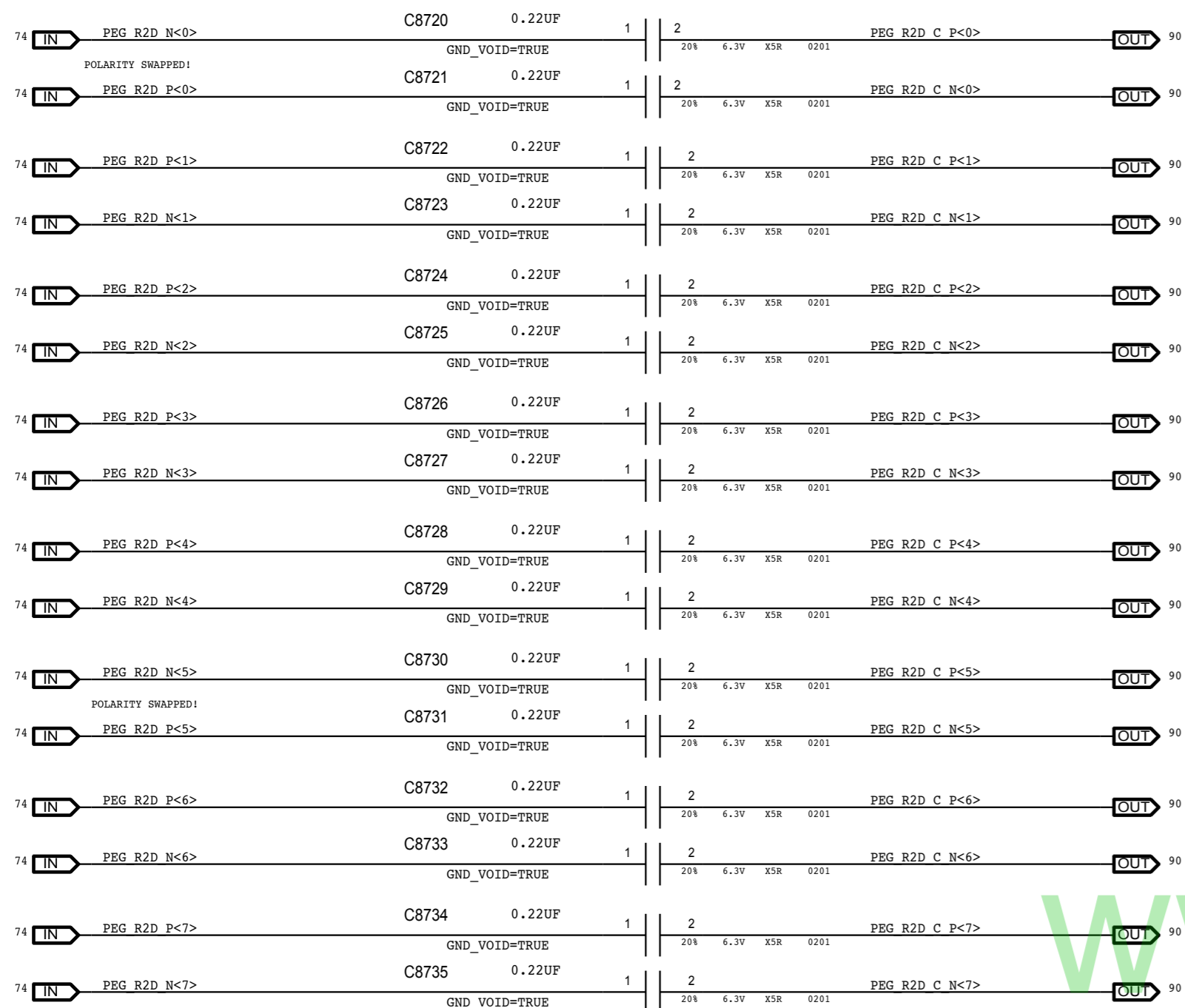
DOI options provided by this page

1908

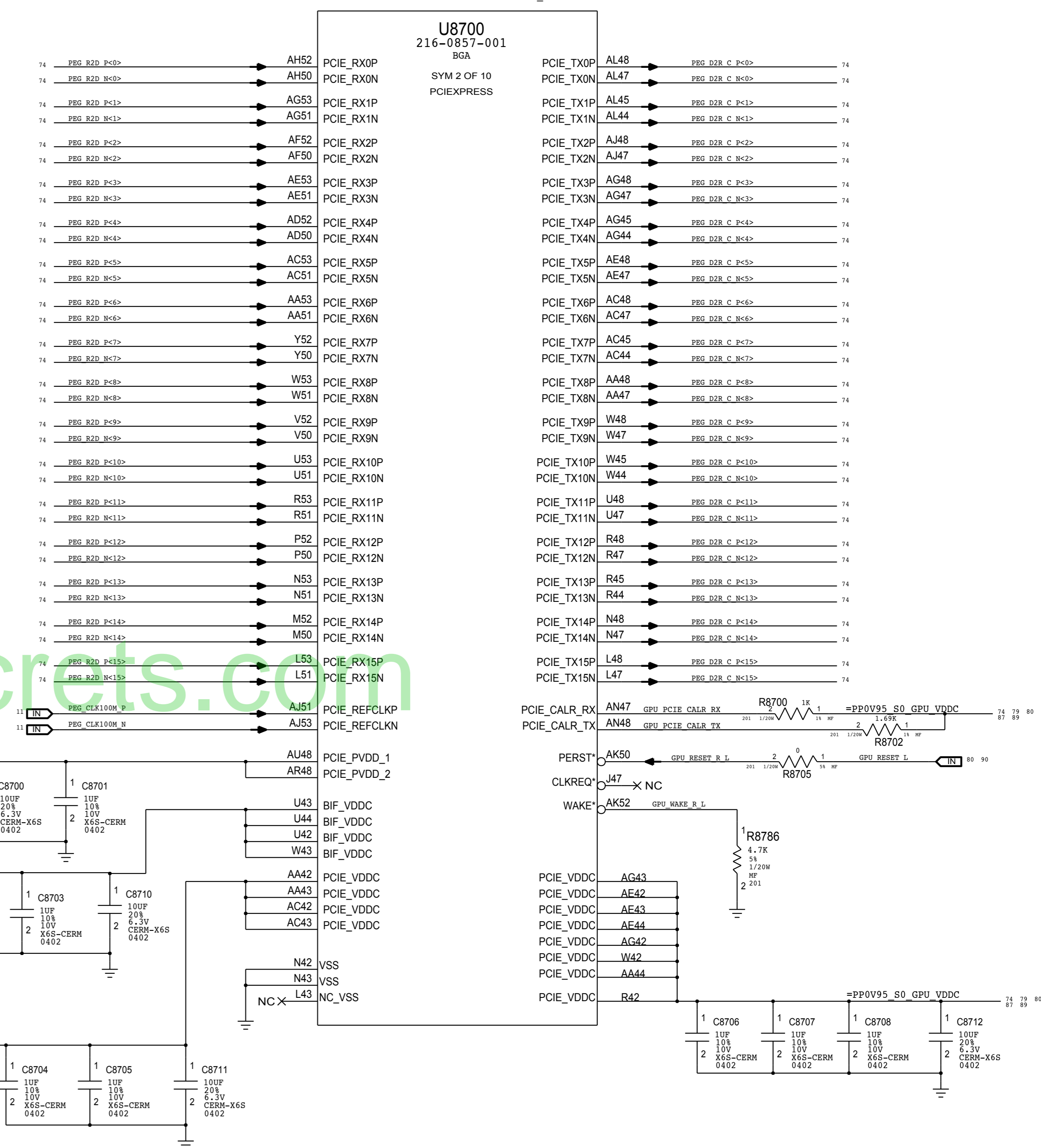
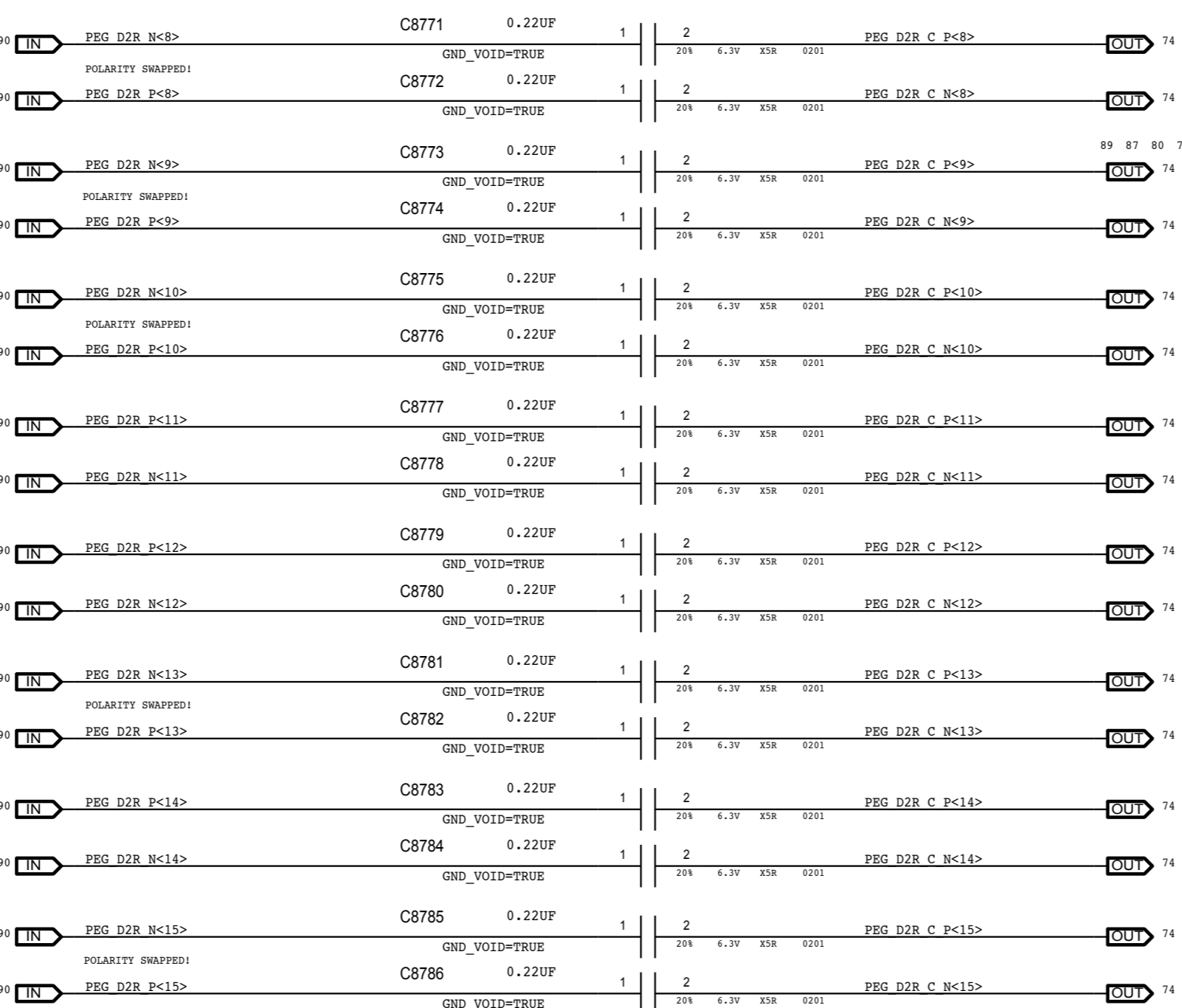
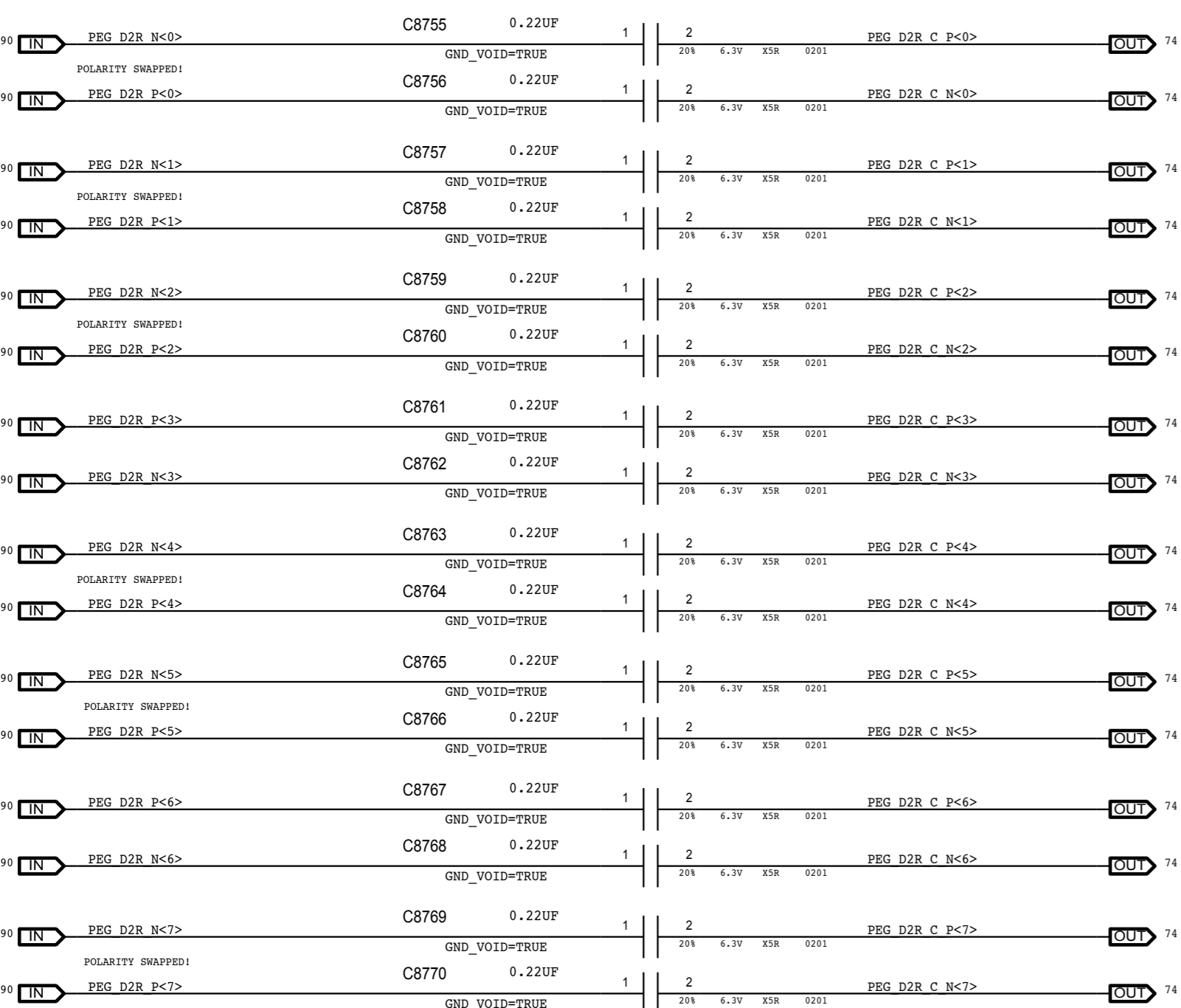
POLARITY SWAPS INTENDED ON LANES,SEE NOTES AT DIFF PAIRS.

ALL LANES ARE ALSO REVERSED, SEE ALIASES ON CSA 112

ALL LANES ARE REVERSED (SEE ALIASES ON CSA 112), SEE DIFF PAIRS FOR POLARITY SWAP INFO



ALL LANES ARE REVERSED (SEE ALIASES ON CSA 112), SEE DIFF PAIRS FOR POLARITY SWAP INFO



SYNC MASTER=J95 SYNC DATE=08/26/2013

PAGE TITLE

GFX: Emerald PCIe



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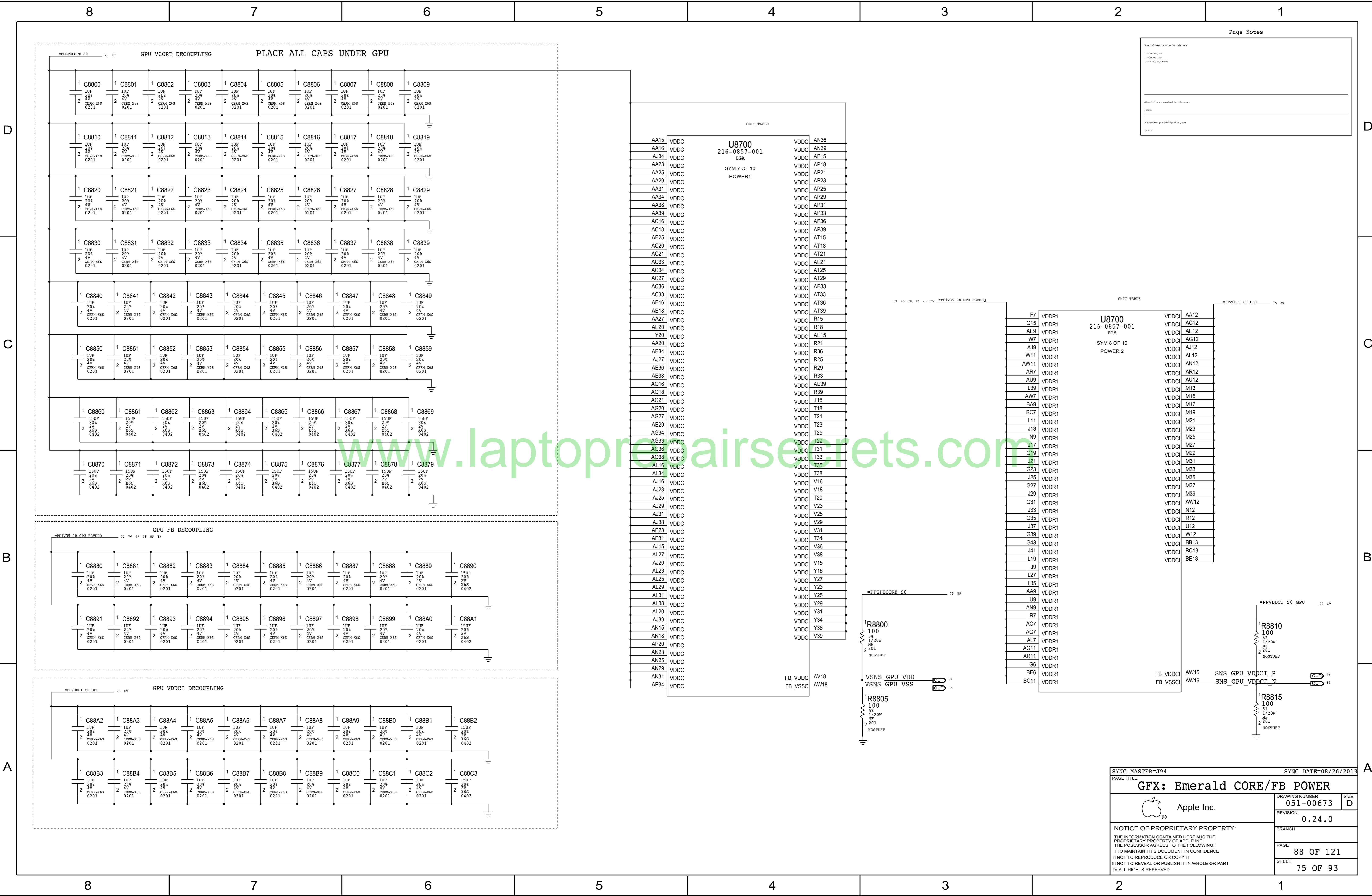
0.24.

BRANCH

PAGE

87 OF 1

SHEET



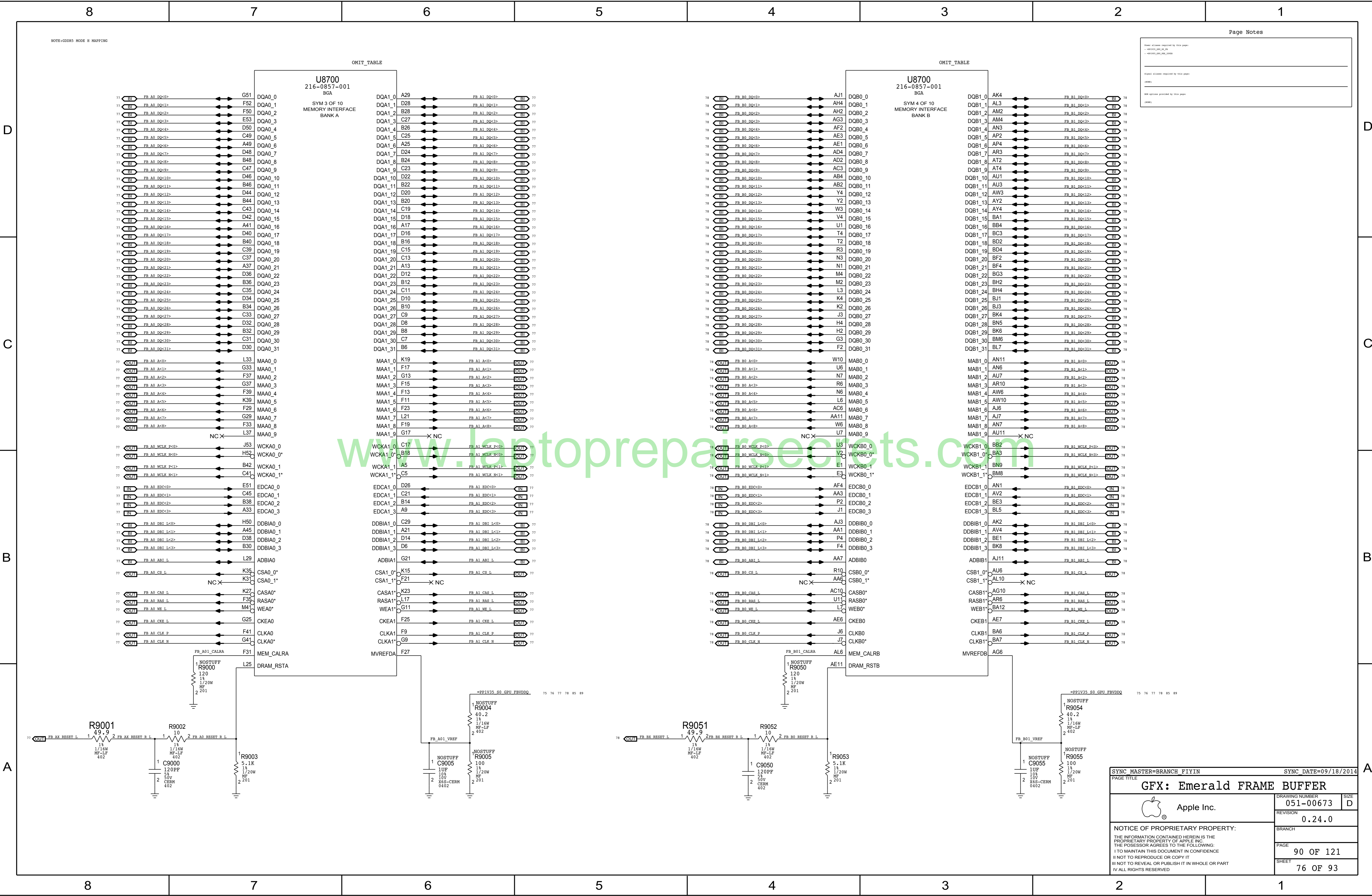
Page Notes

Power: All values required by this page.

Signal: All values required by this page.

See options provided by this page.

|                                                        |  |       |      |
|--------------------------------------------------------|--|-------|------|
| U8700<br>216-0857-001<br>BGA<br>SYM 8 OF 10<br>POWER 2 |  | VDDCI | AA12 |
|                                                        |  | VDDCI | AC12 |
|                                                        |  | VDDCI | AE12 |
|                                                        |  | VDDCI | AG12 |
|                                                        |  | VDDCI | AJ12 |
|                                                        |  | VDDCI | AL12 |
|                                                        |  | VDDCI | AN12 |
|                                                        |  | VDDCI | AR12 |
|                                                        |  | VDDCI | AU12 |
|                                                        |  | VDDCI | M13  |
|                                                        |  | VDDCI | M15  |
|                                                        |  | VDDCI | M17  |
|                                                        |  | VDDCI | M19  |
|                                                        |  | VDDCI | M21  |
|                                                        |  | VDDCI | M23  |
|                                                        |  | VDDCI | M25  |
|                                                        |  | VDDCI | M27  |
|                                                        |  | VDDCI | M29  |
|                                                        |  | VDDCI | M31  |
|                                                        |  | VDDCI | M33  |
|                                                        |  | VDDCI | M35  |
|                                                        |  | VDDCI | M37  |
|                                                        |  | VDDCI | M39  |
|                                                        |  | VDDCI | AW12 |
|                                                        |  | VDDCI | N12  |
|                                                        |  | VDDCI | R12  |
|                                                        |  | VDDCI | U12  |
|                                                        |  | VDDCI | W12  |
|                                                        |  | VDDCI | BB13 |
|                                                        |  | VDDCI | BC13 |
|                                                        |  | VDDCI | BE13 |



Page Notes

Power aliases required by this page:  
- mem01\_000\_000  
- mem01\_000\_000

Signal aliases required by this page:  
(none)

Net aliases provided by this page:  
(none)

SYNC\_MASTER=BRANCH\_FIYN

SYNC\_DATE=09/18/2014

DRAWING NUMBER

051-00673

SIZE

D

REVISION

0.24.0

BRANCH

PAGE

90 OF 121

SHEET

76 OF 93

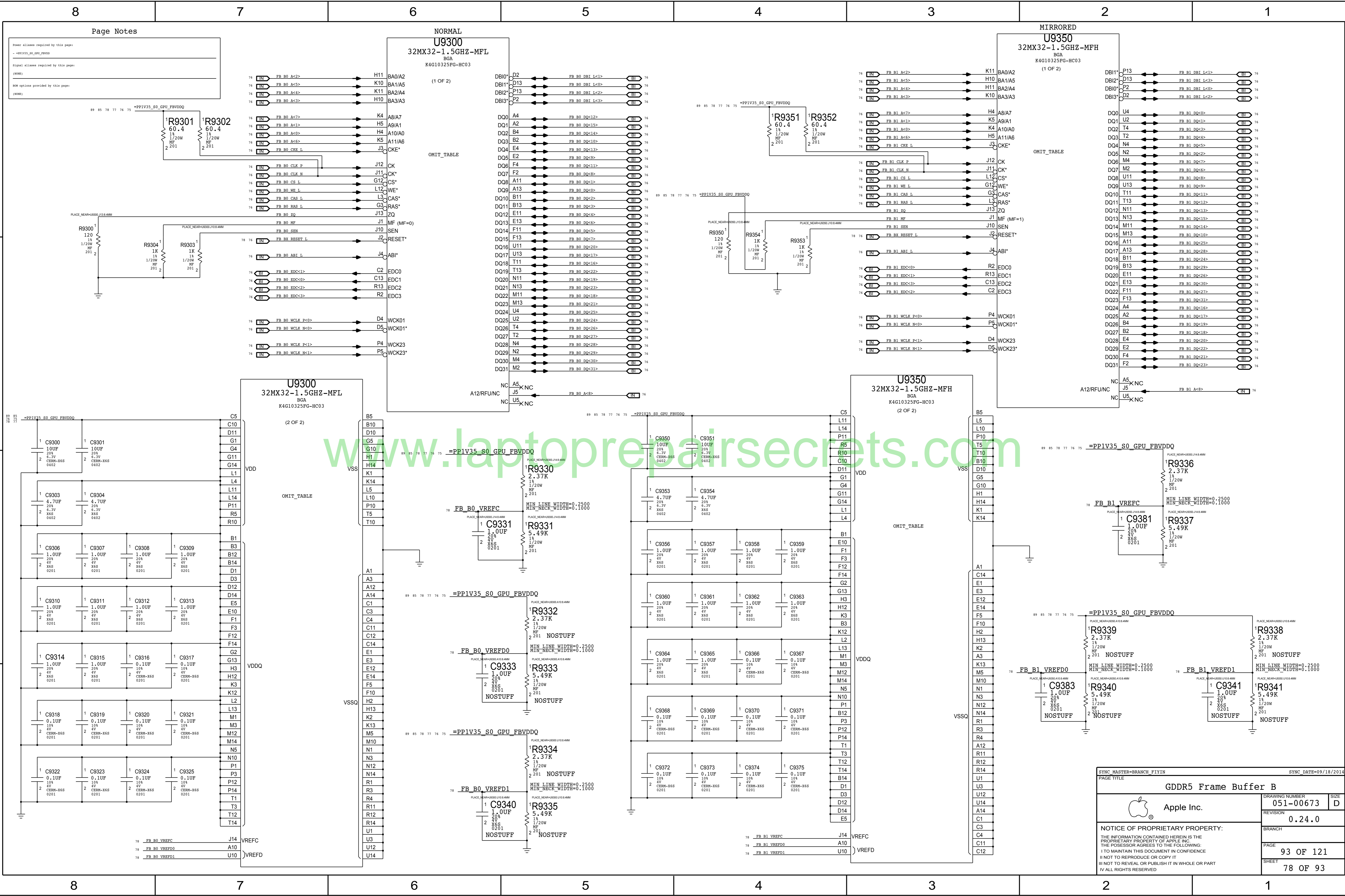
GFX: Emerald FRAME BUFFER

Apple Inc.

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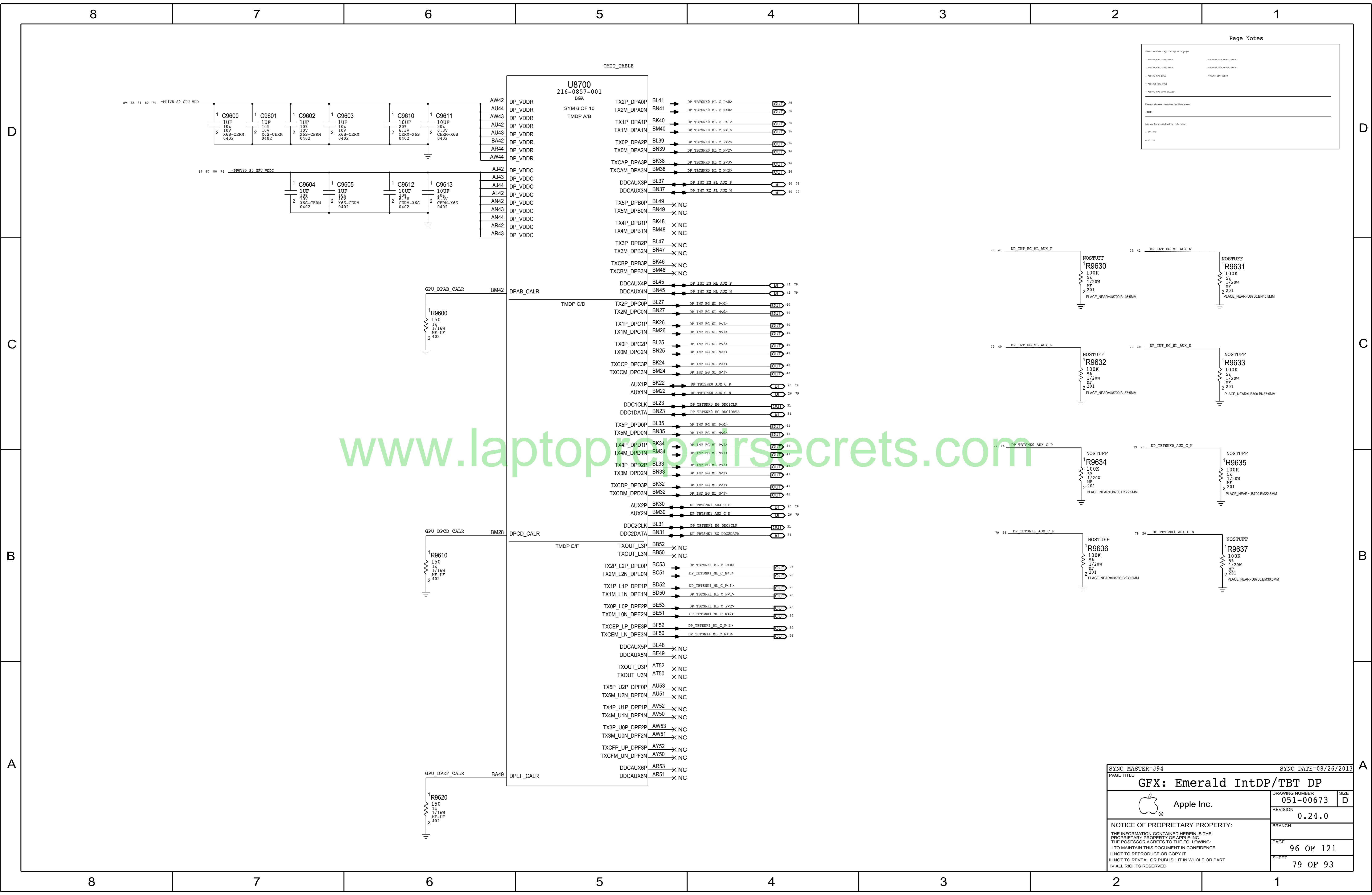
Page Notes

Power aliases required by this page:  
- PP1V35\_S0\_GPU\_FBVDDQ

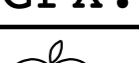
Signal aliases required by this page:  
(NONE)

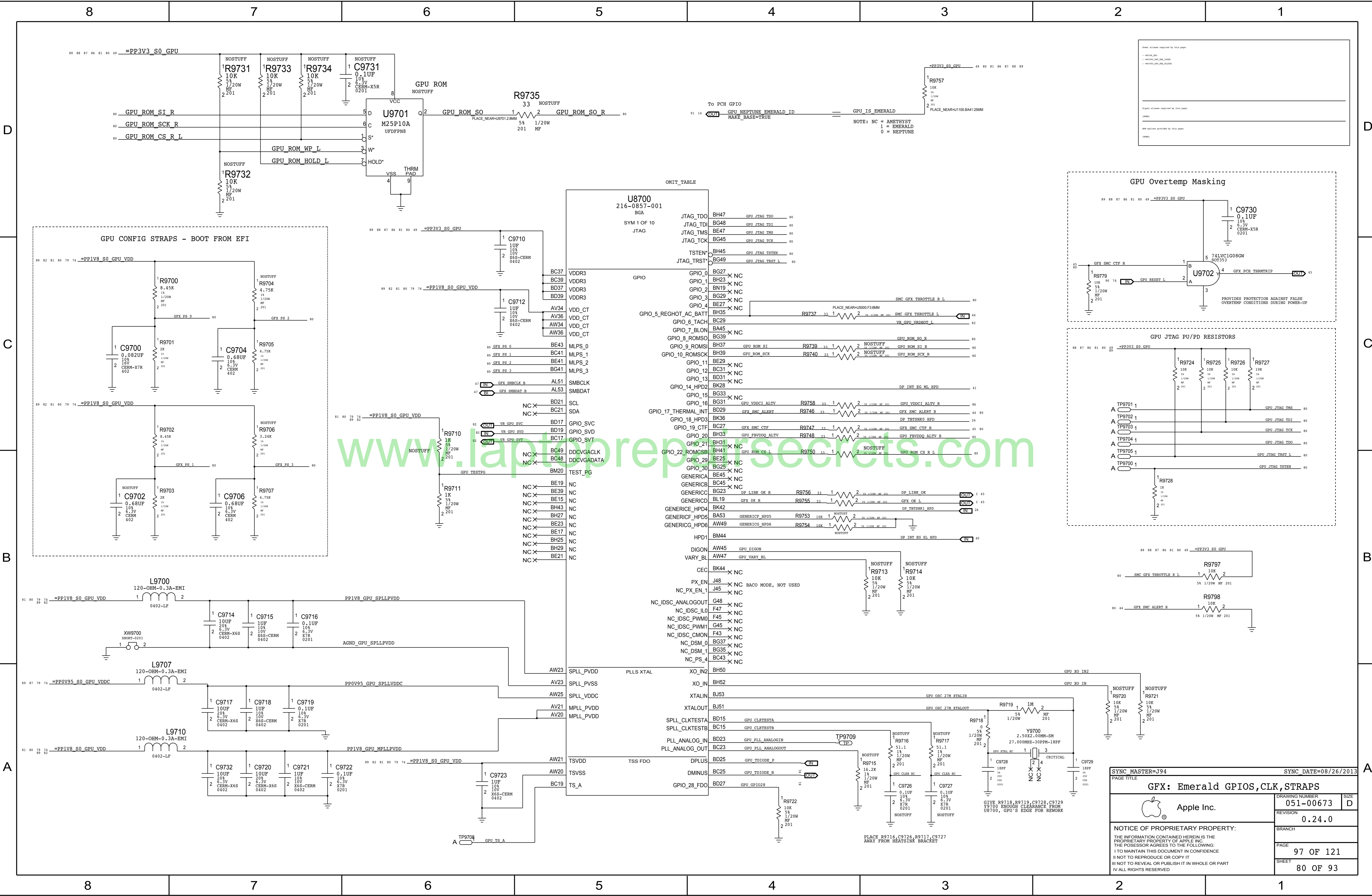
ROM options provided by this page:  
(NONE)

|                                                                                                                                                                                                                                                                                                                   |  |                      |           |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--|----------------------|-----------|
| SYNC_MASTER=BRANCH_FIYIN                                                                                                                                                                                                                                                                                          |  | SYNC_DATE=09/18/2014 |           |
| PAGE TITLE                                                                                                                                                                                                                                                                                                        |  |                      |           |
| GDDR5 Frame Buffer B                                                                                                                                                                                                                                                                                              |  | DRAWING NUMBER       | 051-00673 |
|  Apple Inc.                                                                                                                                                                                                                  |  | REVISION             | 0.24.0    |
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|                                                                                                                                                                                                                                                                                                                   |  | PAGE                 | 93 OF 121 |
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| Page Notes                           |                     |
|--------------------------------------|---------------------|
| Power planes required by this page:  |                     |
| ~ VDDP1_DP_VDD_1000                  | ~ VDDP1_DP_VDD_1000 |
| ~ VDDP1_DP_VDD_1000                  | ~ VDDP1_DP_VDD_1000 |
| ~ VDDP1_DP_VDD_1000                  | ~ VDDP1_DP_VDD_1000 |
| ~ VDDP1_DP_VDD_1000                  | ~ VDDP1_DP_VDD_1000 |
| ~ VDDP1_DP_VDD_1000                  | ~ VDDP1_DP_VDD_1000 |
| ~ VDDP1_DP_VDD_1000                  | ~ VDDP1_DP_VDD_1000 |
| Signal planes required by this page: |                     |
| (NONE)                               |                     |
| SMD options provided by this page:   |                     |
| ~ 251100                             |                     |
| ~ 251100                             |                     |

|                                                                                                                         |            |                      |           |      |
|-------------------------------------------------------------------------------------------------------------------------|------------|----------------------|-----------|------|
| SYNC_MASTER=J94                                                                                                         |            | SYNC_DATE=08/26/2013 |           |      |
| PAGE TITLE                                                                                                              |            |                      |           |      |
| GFX: Emerald IntDP/TBT DP                                                                                               |            |                      |           |      |
|                                    | Apple Inc. | DRAWING NUMBER       | 051-00673 | SIZE |
|                                                                                                                         |            | REVISION             | 0.24.0    |      |
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Power aliases required by this page:

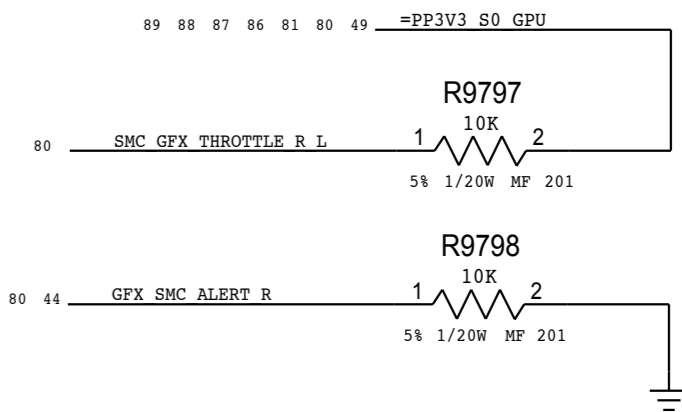
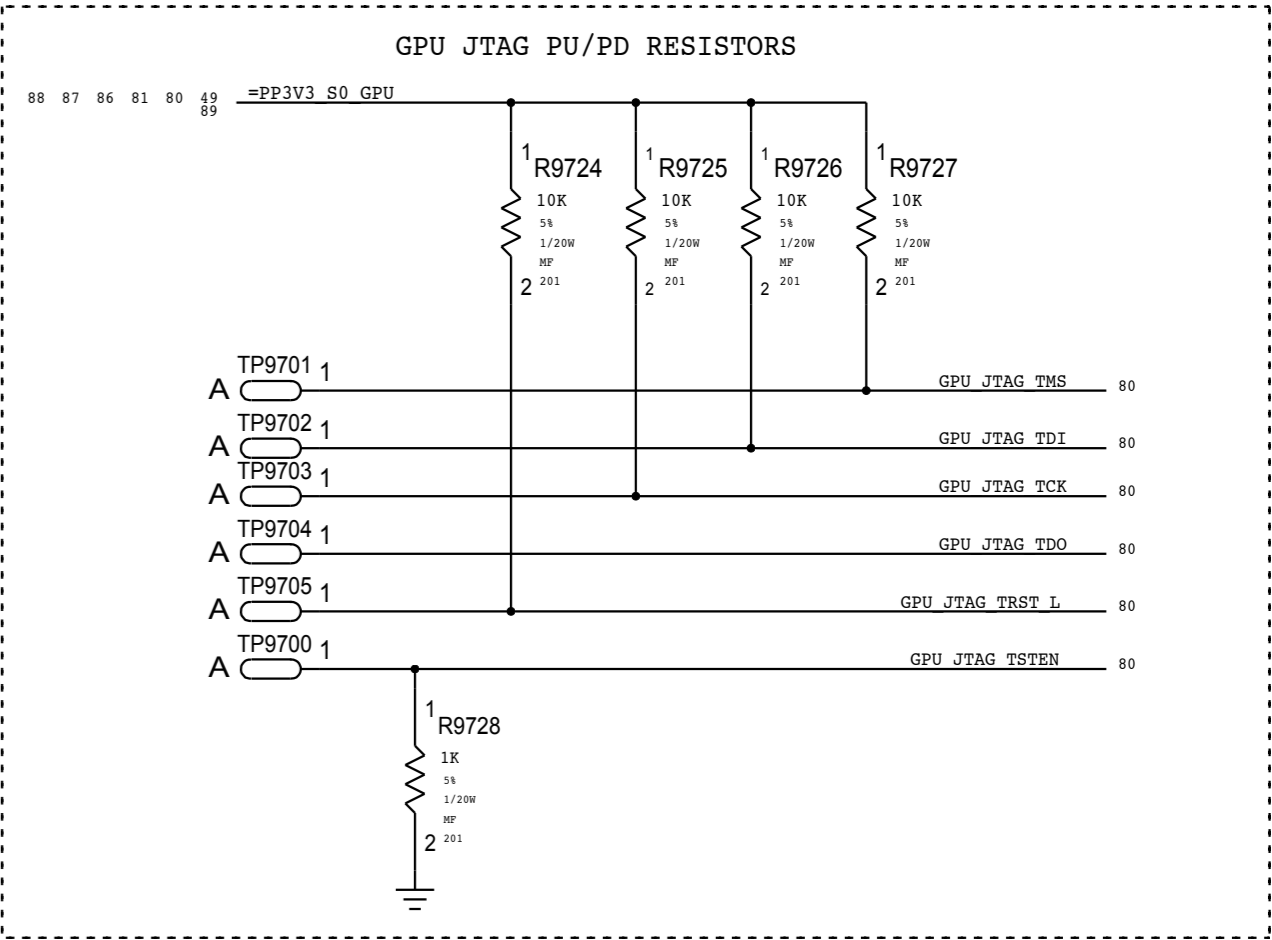
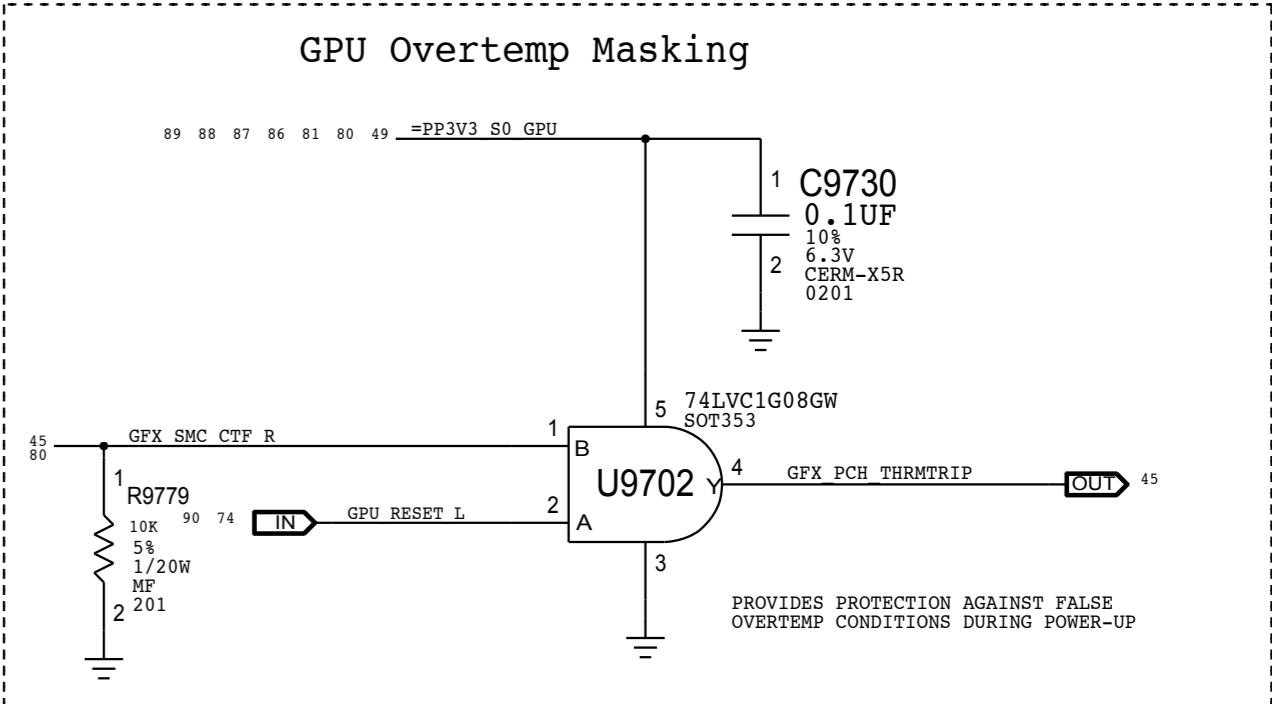
- ~PP3V3\_GPU
- ~PP3V3\_GPU\_ROM\_2000
- ~PP3V3\_GPU\_ROM\_2000

Signal aliases required by this page:

(none)

Non options provided by this page:

(none)



SYNC\_MASTER=J94 SYNC\_DATE=08/26/2013

PAGE TITLE

### GFX: Emerald GPIOs,CLK,STRAPS

Apple Inc.

DRAWING NUMBER 051-00673 SIZE D

REVISION 0.24.0

BRANCH

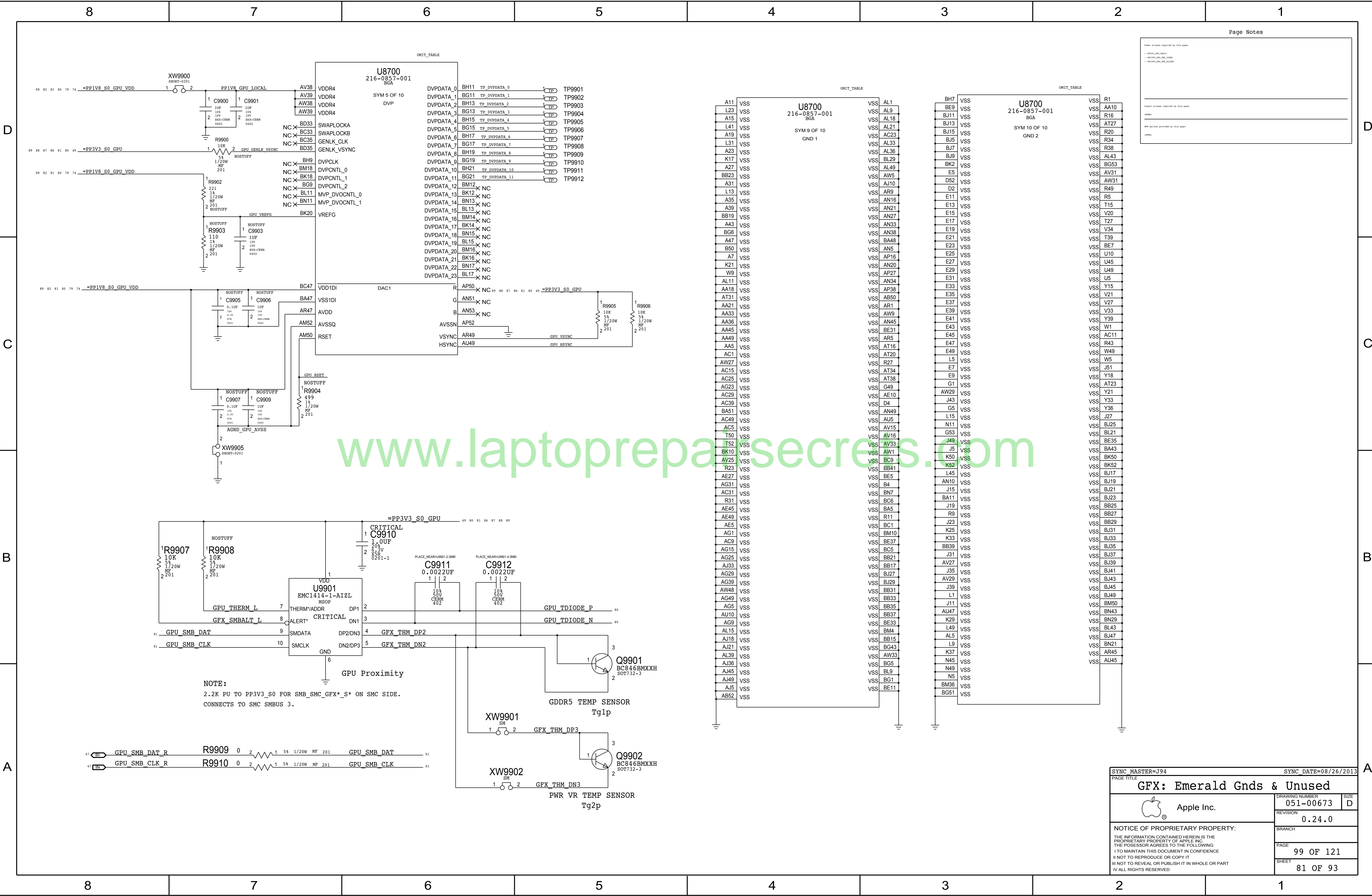
PAGE 97 OF 121

SHEET 80 OF 93

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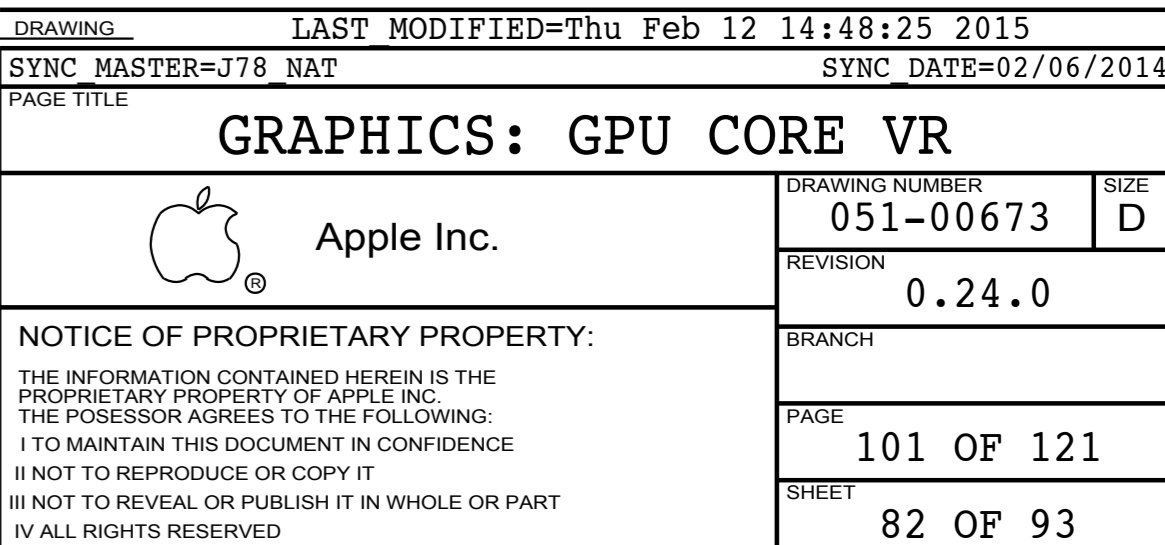
| Page Notes                                    |  |
|-----------------------------------------------|--|
| Power: All values are provided by this page.  |  |
| Signal: All values are provided by this page. |  |
| BOM options provided by this page.            |  |

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NOTE:  
2.2K PU TO PP3V3\_S0 FOR SMB\_SMC GFX\*\_S\* ON SMC SIDE.  
CONNECTS TO SMC SMBUS 3.

|                                                                                                  |  |                      |           |
|--------------------------------------------------------------------------------------------------|--|----------------------|-----------|
| SYNC_MASTER=J94                                                                                  |  | SYNC_DATE=08/26/2013 |           |
| PAGE TITLE                                                                                       |  |                      |           |
| GFX: Emerald Gnds & Unused                                                                       |  |                      |           |
|  Apple Inc. |  | DRAWING NUMBER       | 051-00673 |
|                                                                                                  |  | REVISION             | 0.24.0    |
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GPUCORE  
VOUT = VCORE  
PEAK = 195A  
AVG = 154A



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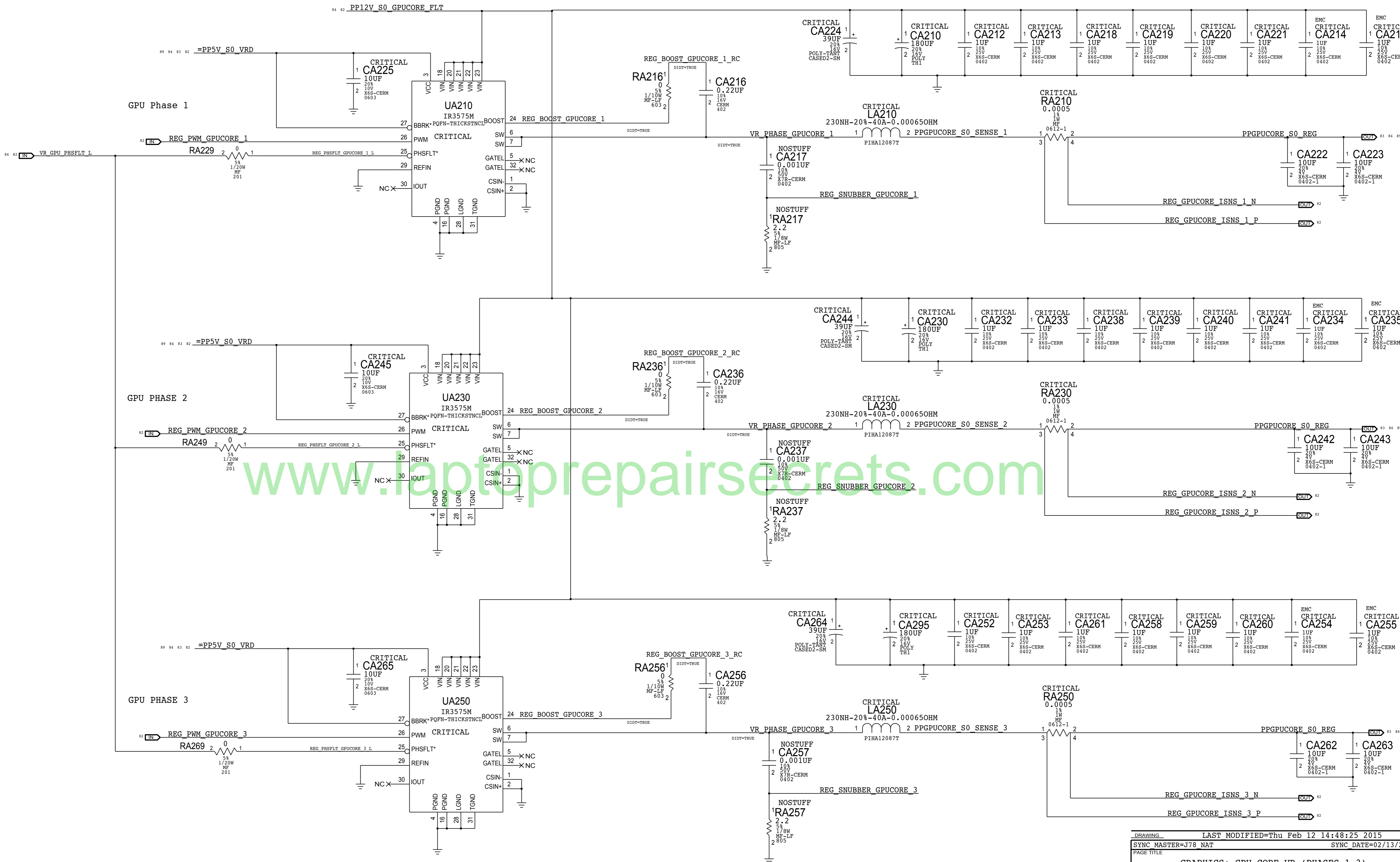
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|                                                                                                                                                                                                                                                                                |                |                                        |      |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------|----------------------------------------|------|
| <u>DRAWING</u>                                                                                                                                                                                                                                                                 |                | LAST MODIFIED=Thu Feb 12 14:48:25 2015 |      |
| SYNC MASTER=J78 NAT                                                                                                                                                                                                                                                            |                | SYNC DATE=02/13/2014                   |      |
| PAGE TITLE                                                                                                                                                                                                                                                                     |                |                                        |      |
| GRAPHICS: GPU CORE VR (PHASES 1-3)                                                                                                                                                                                                                                             |                |                                        |      |
|  Apple Inc.                                                                                                                                                                               | DRAWING NUMBER |                                        | SIZE |
|                                                                                                                                                                                                                                                                                | 051-00673      |                                        | D    |
|                                                                                                                                                                                                                                                                                | REVISION       |                                        |      |
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|                                                                                                                                                                                                                                                                                |                | 102 OF 121                             |      |
|                                                                                                                                                                                                                                                                                |                | SHEET                                  |      |
|                                                                                                                                                                                                                                                                                |                | 83 OF 93                               |      |

D

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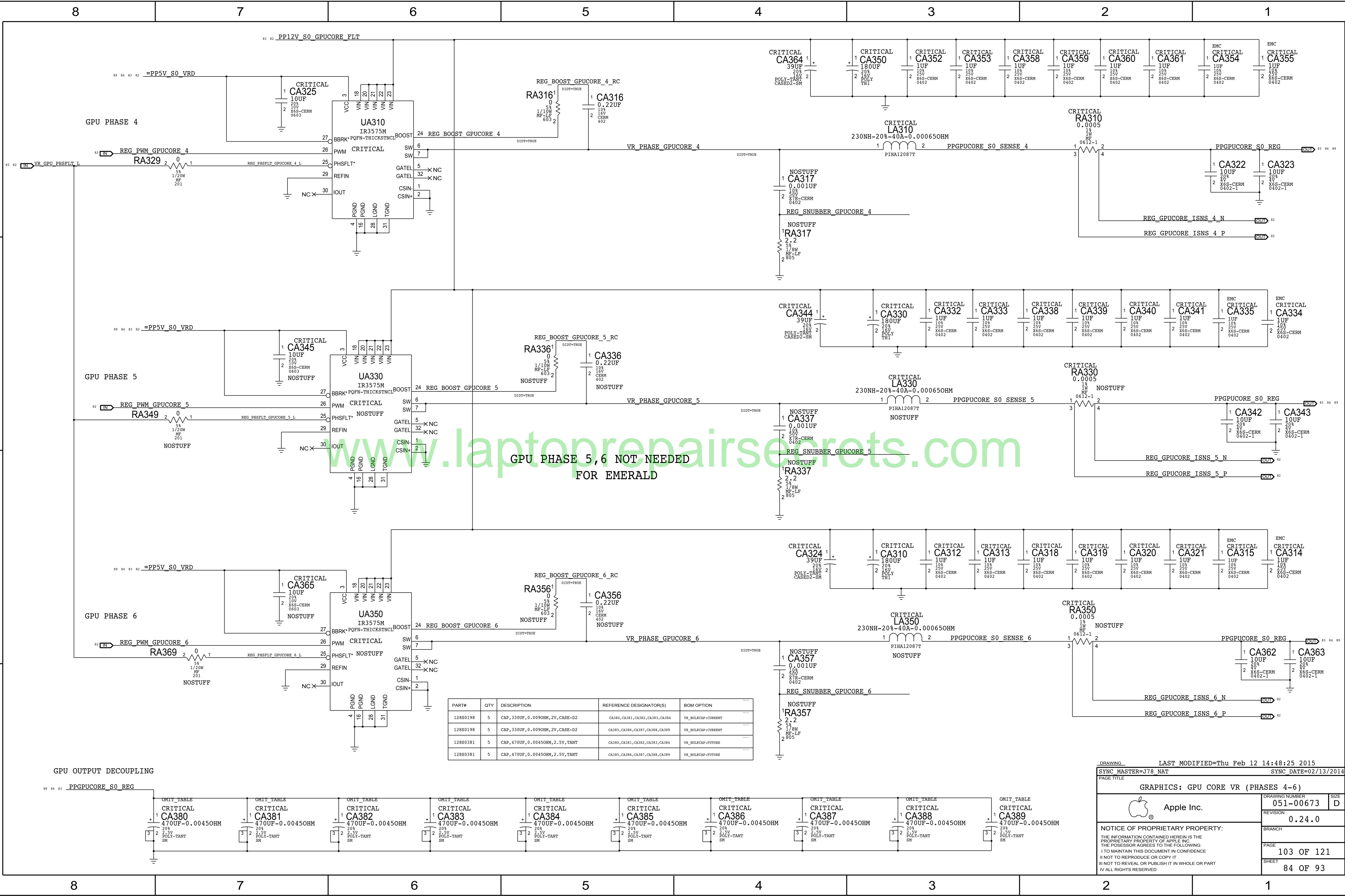
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| PART#    | QTY | DESCRIPTION                       | REFERENCE DESIGNATOR(S)           | BOM OPTION         |
|----------|-----|-----------------------------------|-----------------------------------|--------------------|
| 128S0198 | 5   | CAP, 330UF, 0.0090HM, 2V, CASE-D2 | CA380, CA381, CA382, CA383, CA384 | VR_BULKCAP:CURRENT |
| 128S0198 | 5   | CAP, 330UF, 0.0090HM, 2V, CASE-D2 | CA385, CA386, CA387, CA388, CA389 | VR_BULKCAP:CURRENT |
| 128S0381 | 5   | CAP, 470UF, 0.00450HM, 2.5V, TANT | CA380, CA381, CA382, CA383, CA384 | VR_BULKCAP:FUTURE  |
| 128S0381 | 5   | CAP, 470UF, 0.00450HM, 2.5V, TANT | CA385, CA386, CA387, CA388, CA389 | VR_BULKCAP:FUTURE  |

DRAWING


LAST MODIFIED=Thu Feb 12 14:48:25 2015

SYNC MASTER=J78 NAT

SYNC DATE=02/13/2014

PAGE TITLE

GRAPHICS: GPU CORE VR (PHASES 4-6)

 Apple Inc.

DRAWING NUMBER

051-00673

SIZE

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REVISION

0.24.0

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PAGE

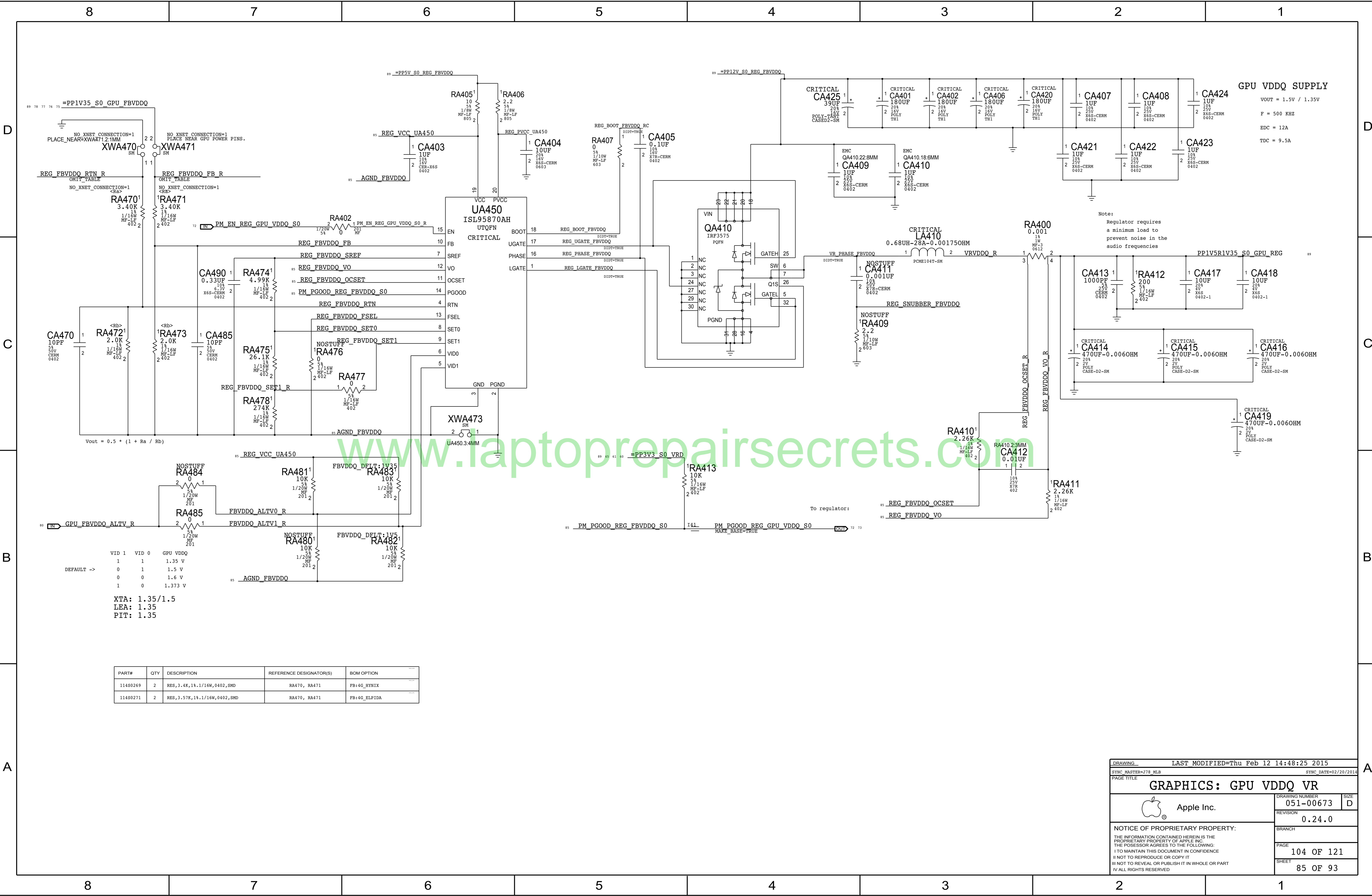
103 OF 121


SHEET

84 OF 93

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| DRAWING                                                                                                                                                                                                                                                                                                                  |  | LAST MODIFIED=Thu Feb 12 14:48:25 2015 |  |
| SYNC_MASTER=J78_MLB                                                                                                                                                                                                                                                                                                      |  | SYNC_DATE=02/20/2014                   |  |
| PAGE TITLE                                                                                                                                                                                                                                                                                                               |  |                                        |  |
| GRAPHICS: GPU VDDQ VR                                                                                                                                                                                                                                                                                                    |  |                                        |  |
|  Apple Inc.                                                                                                                                                                                                                         |  | DRAWING NUMBER                         |  |
|                                                                                                                                                                                                                                                                                                                          |  | 051-00673                              |  |
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|                                                                                                                                                                                                                                                                                                                          |  | PAGE                                   |  |
|                                                                                                                                                                                                                                                                                                                          |  | 104 OF 121                             |  |
|                                                                                                                                                                                                                                                                                                                          |  | SHEET                                  |  |
|                                                                                                                                                                                                                                                                                                                          |  | 85 OF 93                               |  |

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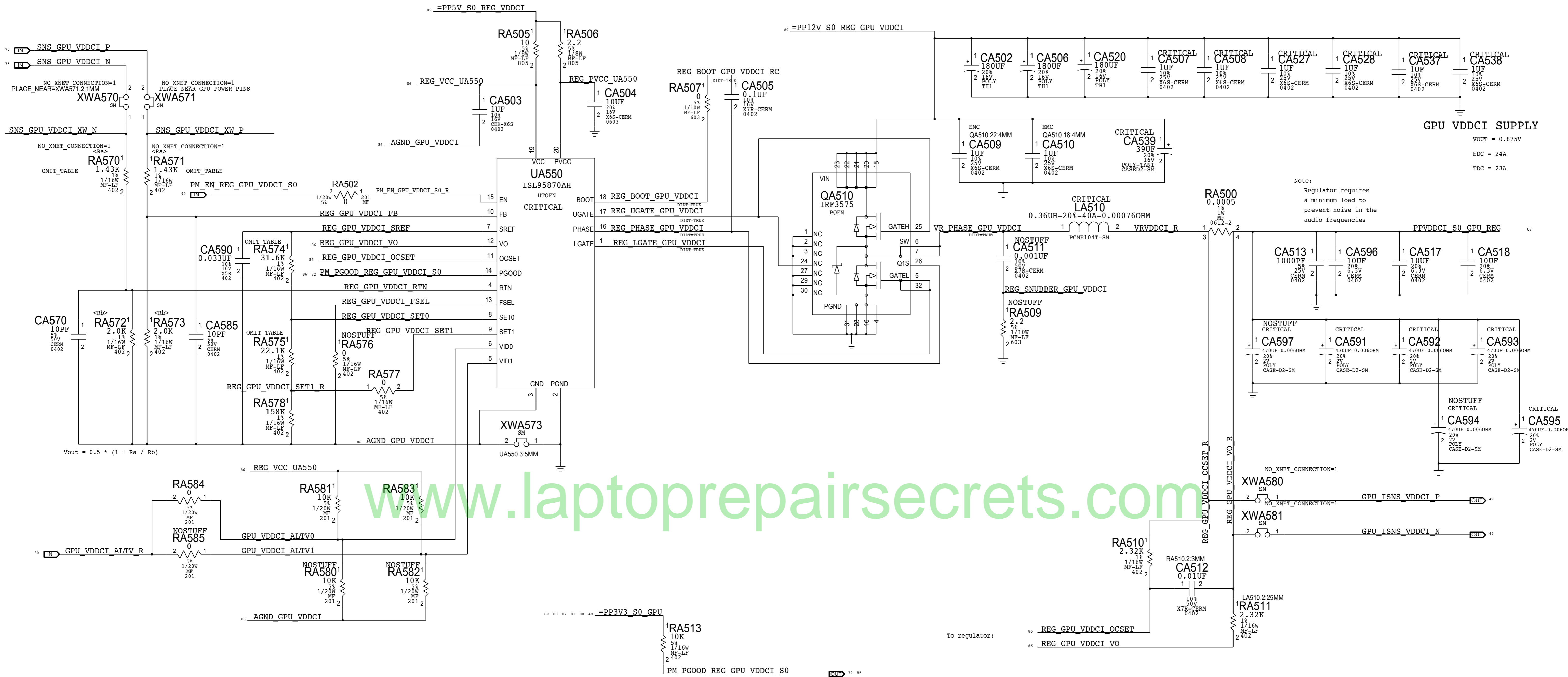
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| NEPTUNE    |       |       |           | AMETHYST   |       |       |           |
|------------|-------|-------|-----------|------------|-------|-------|-----------|
|            | VID 1 | VID 0 | GPU VDDCI |            | VID 1 | VID 0 | GPU VDDCI |
| DEFAULT -> | 1     | 1     | 0.850 V   | DEFAULT -> | 1     | 1     | 0.900 V   |
|            | 1     | 0     | 1.000 V   |            | 1     | 0     | 1.000 V   |


| PART#    | QTY | DESCRIPTION    | REFERENCE DESIGNATOR(S) | BOM OPTION         |
|----------|-----|----------------|-------------------------|--------------------|
| 11480363 | 1   | RES,31.6K,0402 | RA574                   | GPU_Emerald        |
| 11680068 | 2   | RES,1.2K,0402  | RA570,RA571             | GPU_Emerald        |
| 11480378 | 1   | RES,45.3K,0402 | RA575                   | GPU_Emerald        |
| 11480363 | 1   | RES,31.6K,0402 | RA574                   | GPU_Neptune        |
| 11480231 | 2   | RES,1.4K,0402  | RA570,RA571             | GPU_Neptune        |
| 11480347 | 1   | RES,22.1K,0402 | RA575                   | GPU_Neptune        |
| 11480373 | 1   | RES,40.2K,0402 | RA574                   | GPU_AmethystP_XTA  |
| 11480228 | 2   | RES,1.3K,0402  | RA570,RA571             | GPU_AmethystP_XTA  |
| 11480347 | 1   | RES,22.1K,0402 | RA575                   | GPU_AmethystP_XTA  |
| 11480382 | 1   | RES,48.7K,0402 | RA574                   | GPU_AmethystP_PROA |
| 11480228 | 2   | RES,1.3K,0402  | RA570,RA571             | GPU_AmethystP_PROA |
| 11480347 | 1   | RES,22.1K,0402 | RA575                   | GPU_AmethystP_PROA |

SYNC\_MASTER=hcheng\_j95

SYNC\_DATE=02/10/2015

PAGE TITLE

GRAPHICS: GPU VDDCI VR

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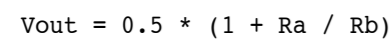
PAGE

105 OF 121

SHEET

86 OF 93

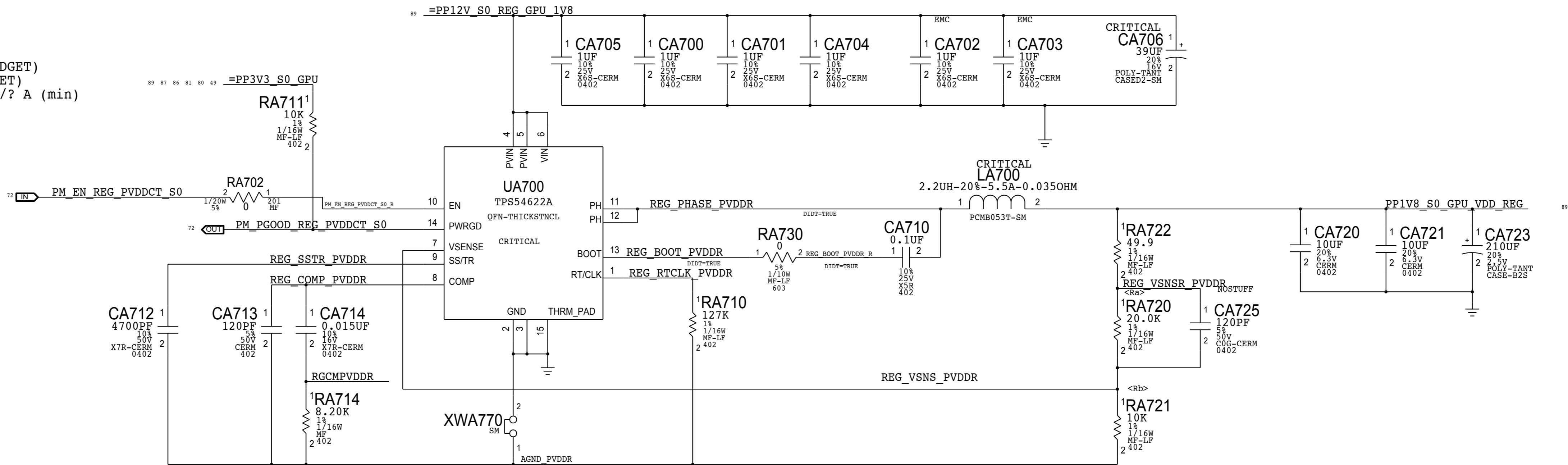
Max avg current: 4.3 A  
Max peak current: 4.5 A  
Switching freq: 300 kHz



| PART#    | QTY | DESCRIPTION                     | REFERENCE DESIGNATOR(S) | BOM OPTION         |
|----------|-----|---------------------------------|-------------------------|--------------------|
| 128S0358 | 2   | CAP, 470uF, 0.0060HM, 2V, D2    | CA640, CA641            | VR_BULKCAP:CURRENT |
| 128S0381 | 2   | CAP, 470uF, 0.00450HM, 2.5V, SM | CA640, CA641            | VR_BULKCAP:FUTURE  |


1.8V S0 Regulator

Max avg current: 2.4 A (BUDGET)  
Max peak current: 3 A (BUDGET)  
OC trip point: ? A (nom)/? A (min)  
Switching freq: ? kHz



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$$V_{OUT} = 0.6 \cdot (1 + R_A / R_B)$$

|                                                                                                                                                                                                                                                                                                                      |                |                                        |            |      |   |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------|----------------------------------------|------------|------|---|
| DRAWING                                                                                                                                                                                                                                                                                                              |                | LAST MODIFIED=Thu Feb 12 14:48:26 2015 |            |      |   |
| SYNC_MASTER=J95_HARPER                                                                                                                                                                                                                                                                                               |                | SYNC_DATE=02/11/2015                   |            |      |   |
| PAGE TITLE                                                                                                                                                                                                                                                                                                           |                |                                        |            |      |   |
| GRAPHICS: GPU 1V8 VR                                                                                                                                                                                                                                                                                                 |                |                                        |            |      |   |
|  Apple Inc.                                                                                                                                                                                                                     | DRAWING NUMBER |                                        | 051-00673  | SIZE | D |
|                                                                                                                                                                                                                                                                                                                      | REVISION       |                                        | 0.24.0     |      |   |
|                                                                                                                                                                                                                                                                                                                      | BRANCH         |                                        |            |      |   |
|                                                                                                                                                                                                                                                                                                                      | PAGE           |                                        | 107 OF 121 |      |   |
|                                                                                                                                                                                                                                                                                                                      | SHEET          |                                        | 88 OF 93   |      |   |
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## PEG aliases

|    |                    |                |    |                     |   |
|----|--------------------|----------------|----|---------------------|---|
| 74 | PEG_D2R N<0..15>   | MAKE_BASE=TRUE | == | =PEG_D2R N<15..0>   | 5 |
| 74 | PEG_D2R P<0..15>   | MAKE_BASE=TRUE | == | =PEG_D2R P<15..0>   | 5 |
| 74 | PEG_R2D C N<0..15> | MAKE_BASE=TRUE | == | =PEG_R2D C N<15..0> | 5 |
| 74 | PEG_R2D C P<0..15> | MAKE_BASE=TRUE | == | =PEG_R2D C P<15..0> | 5 |

## GPU ALIASES

```

80 74 GPU_RESET_L _____ TP GPU_RESET_L 19
 MAKE_BASE=TRUE _____
82 VR_GPU_RESET_L _____ TP VR_GPU_RESET_L 19
 MAKE_BASE=TRUE _____

```

```
GPU VDDCI PGOOD
```

```

72 TP PM EN REG GPU VDDCI S0 — PM EN REG GPU VDDCI S0 86
 MAKE BASE=TRUE

```


|   |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |   |   |   |   |   |   |   |   |
|---|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---|---|---|---|---|---|---|---|
|   | 8                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | 7 | 6 | 5 | 4 | 3 | 2 | 1 |   |
| D | <div>CPU Reserved</div> <div><div><div>176CPU_CFG&lt;15..12&gt;====TP_CPU_CFG&lt;15..12&gt;<br/>MAKE_BASE=TRUE</div><div>40_DP_INT_PIN_57====NC_DP_INT_PIN_57<br/>MAKE_BASE=TRUE</div><div>40_DP_INT_PIN_55====NC_DP_INT_PIN_55<br/>MAKE_BASE=TRUE</div></div><div><div>12_TP_CLINK_DATA====CLINK_DATA<br/>MAKE_BASE=TRUENO_TEST=1</div><div>12_TP_CLINK_CLK====CLINK_CLK<br/>MAKE_BASE=TRUENO_TEST=1</div><div>12_TP_CLINK_RESET_L====CLINK_RESAT_L<br/>MAKE_BASE=TRUENO_TEST=1</div><div>TP_GPU_CB_REFCKN_OUT1====GPU_CB_REFCKN_OUT1<br/>MAKE_BASE=TRUE</div><div>TP_GPU_CB_REFCKP_OUT1====GPU_CB_REFCKP_OUT1<br/>MAKE_BASE=TRUE</div><div>TP_GPU_PLL_ANALOG_IN====GPU_PLL_ANALOG_IN<br/>MAKE_BASE=TRUE</div><div>12_TP_PCH_SLP_LAN_L====PCH_SLP_LAN_L<br/>MAKE_BASE=TRUENO_TEST=1</div><div>11_TP_PCH_2====PCH_2<br/>MAKE_BASE=TRUENO_TEST=1</div><div>12_TP_PM_SLP_A_L====PM_SLP_A_L<br/>MAKE_BASE=TRUENO_TEST=1</div><div>26_TP_TBT_MONDC1====TBT_MONDC1<br/>MAKE_BASE=TRUE</div><div>26_TP_TBT_PCIE_RESETO_L====TBT_PCIE_RESETO_L<br/>MAKE_BASE=TRUENO_TEST=1</div></div></div> <div>PCH Clocks</div> <div><div><div>TP_ITPXDP_CLK100MP====ITPXDP_CLK100M_P<br/>MAKE_BASE=TRUENO_TEST=11117</div><div>TP_ITPXDP_CLK100MN====ITPXDP_CLK100M_N<br/>MAKE_BASE=TRUENO_TEST=11117</div></div></div> <div>PCH Miscellaneous</div> <div><div><div>11_TP_HDA_SDIN1====NC_HDA_SDIN1<br/>MAKE_BASE=TRUENO_TEST=1</div><div>11_PEG_CLKREQ_L====NC_PEG_CLKREQ_L<br/>MAKE_BASE=TRUE</div><div>8014_GPU_NEPTUNE_EMERALD_ID====NC_GPU_IS_AMETHYST<br/>MAKE_BASE=TRUENO_TEST=1</div></div></div> |   |   |   |   |   |   |   | D |
| C |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |   |   |   |   |   |   |   | C |
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PAGE TITLE

Unused Signal Aliases



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BRANCH


PAGE

115 OF 121

SHEET

91 OF 93

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|                                                                                                                                                                                                                                                                                                                             | PAGE           |                      | 115 OF 121 |
|                                                                                                                                                                                                                                                                                                                             | SHEET          |                      | 91 OF 93   |



